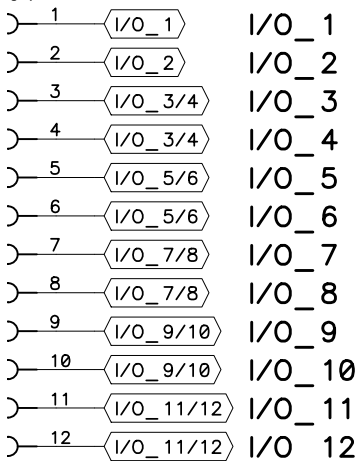
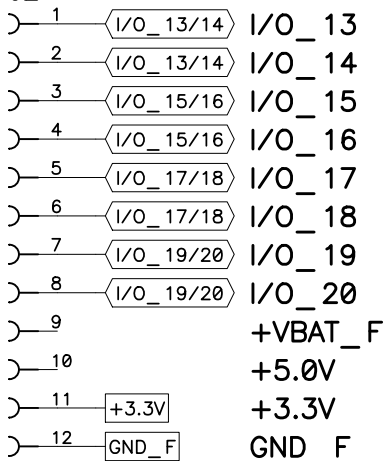


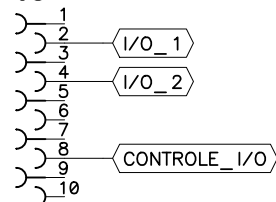
J1



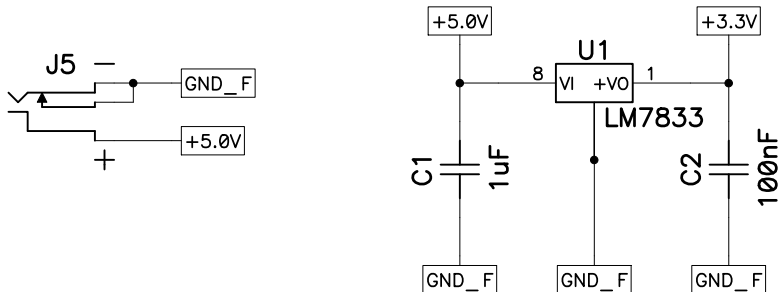
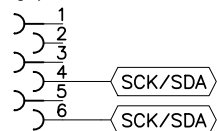
J2



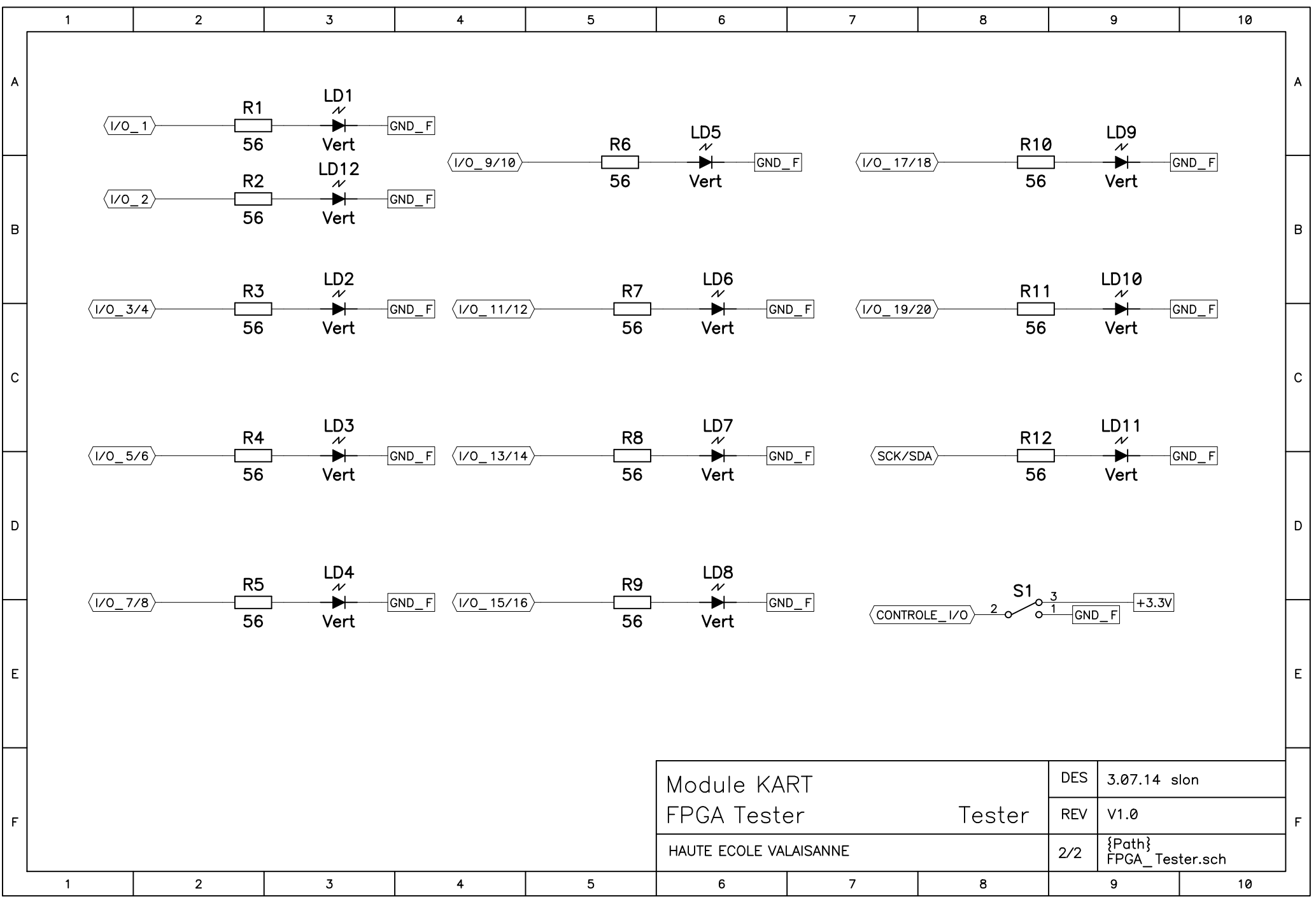
J3



J4



Module KART FPGA Tester	DES	3.07.14 slon
	REV	V1.0
HAUTE ECOLE VALAISANNE	1/2	{Path} FPGA_Tester.sch



Module KART FPGA Tester	DES	3.07.14 slon
	REV	V1.0
HAUTE ECOLE VALAISANNE	2/2	{Path} FPGA_Tester.sch