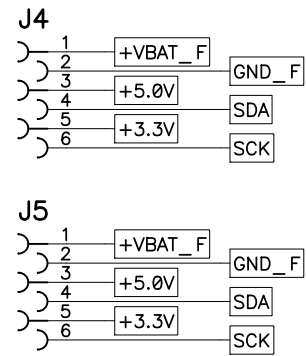
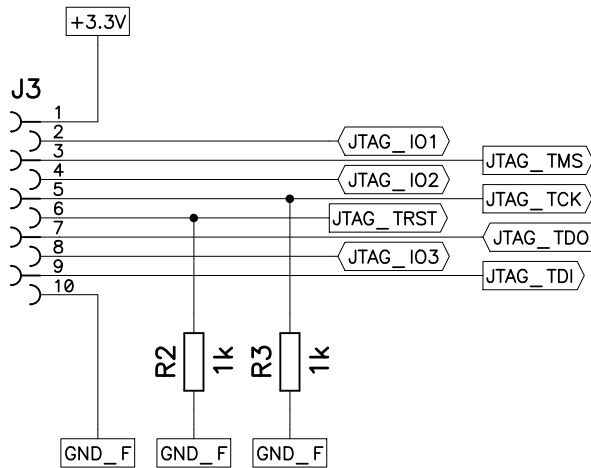
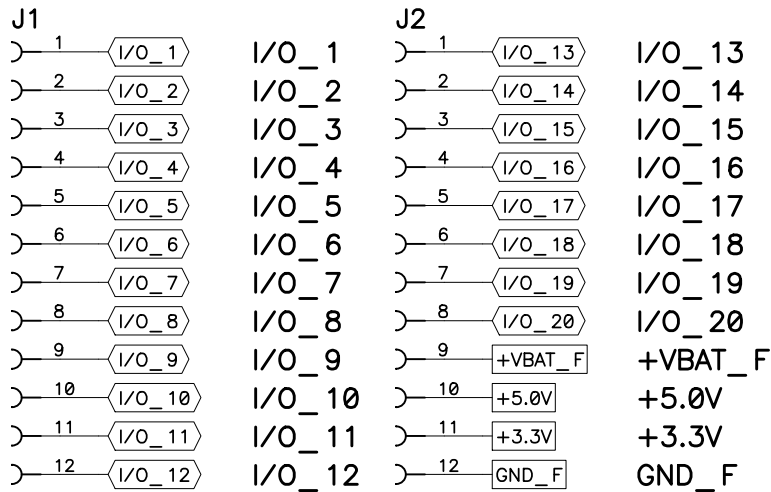
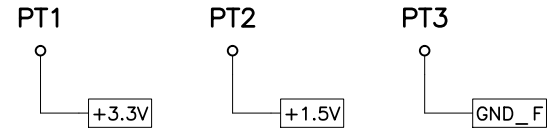
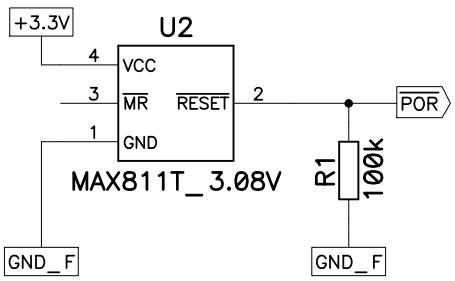
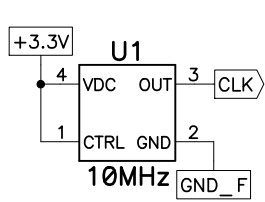


FPGA PROG



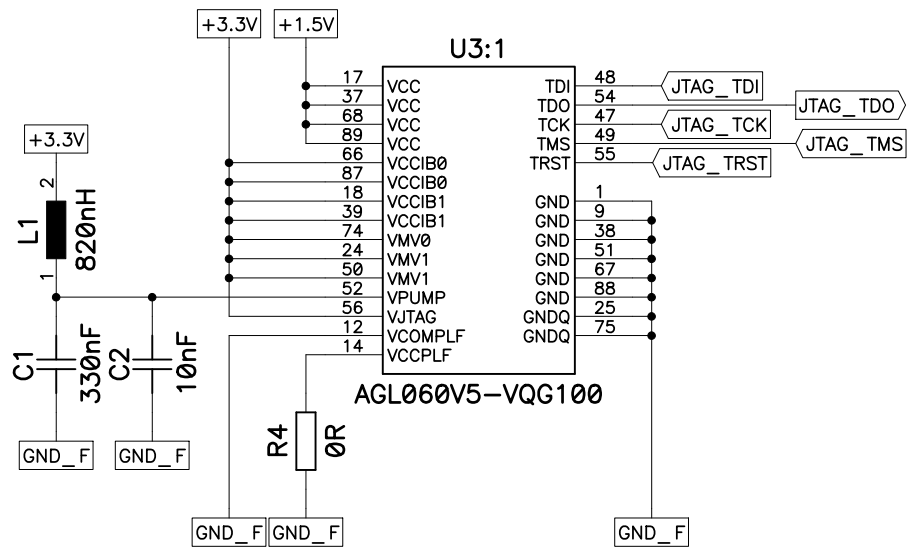
FPGA CLOCK

FPGA RESET

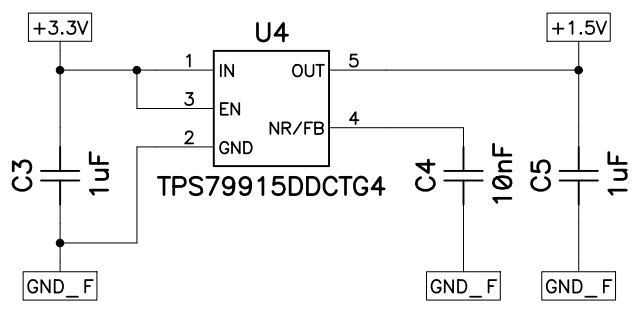


Module KART Control	DES	03.03.2014 WAL
	REV	V4.0
HAUTE ECOLE VALAISANNE	1/3	{Path} Kart_Control_V40.SCH

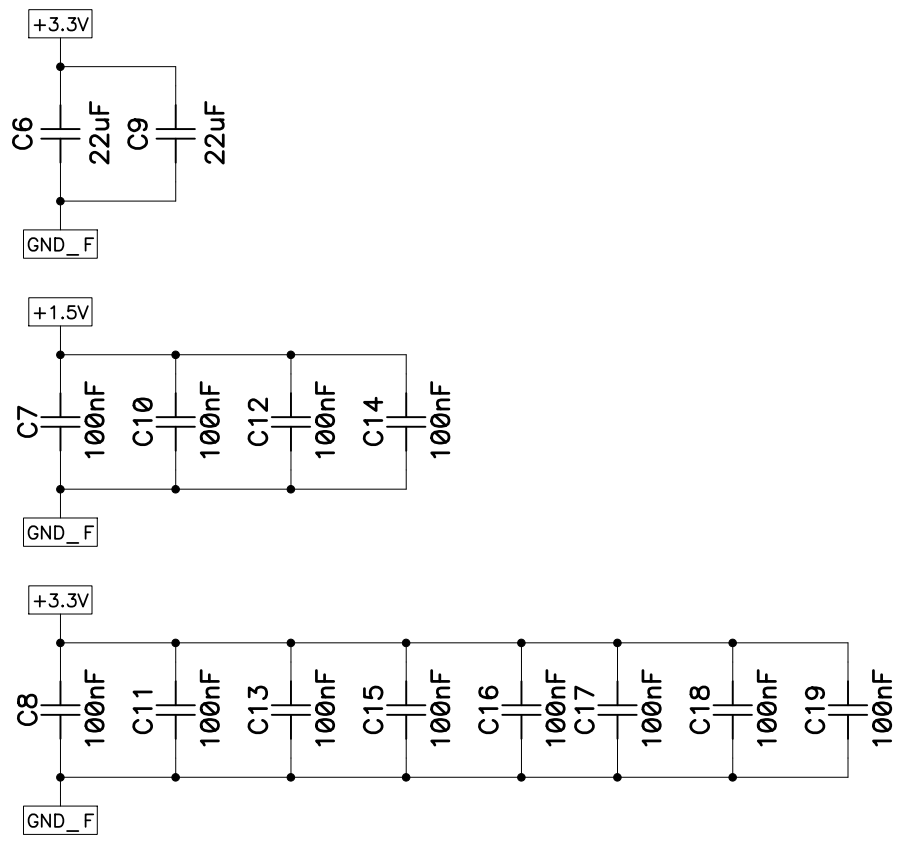
FPGA POWER



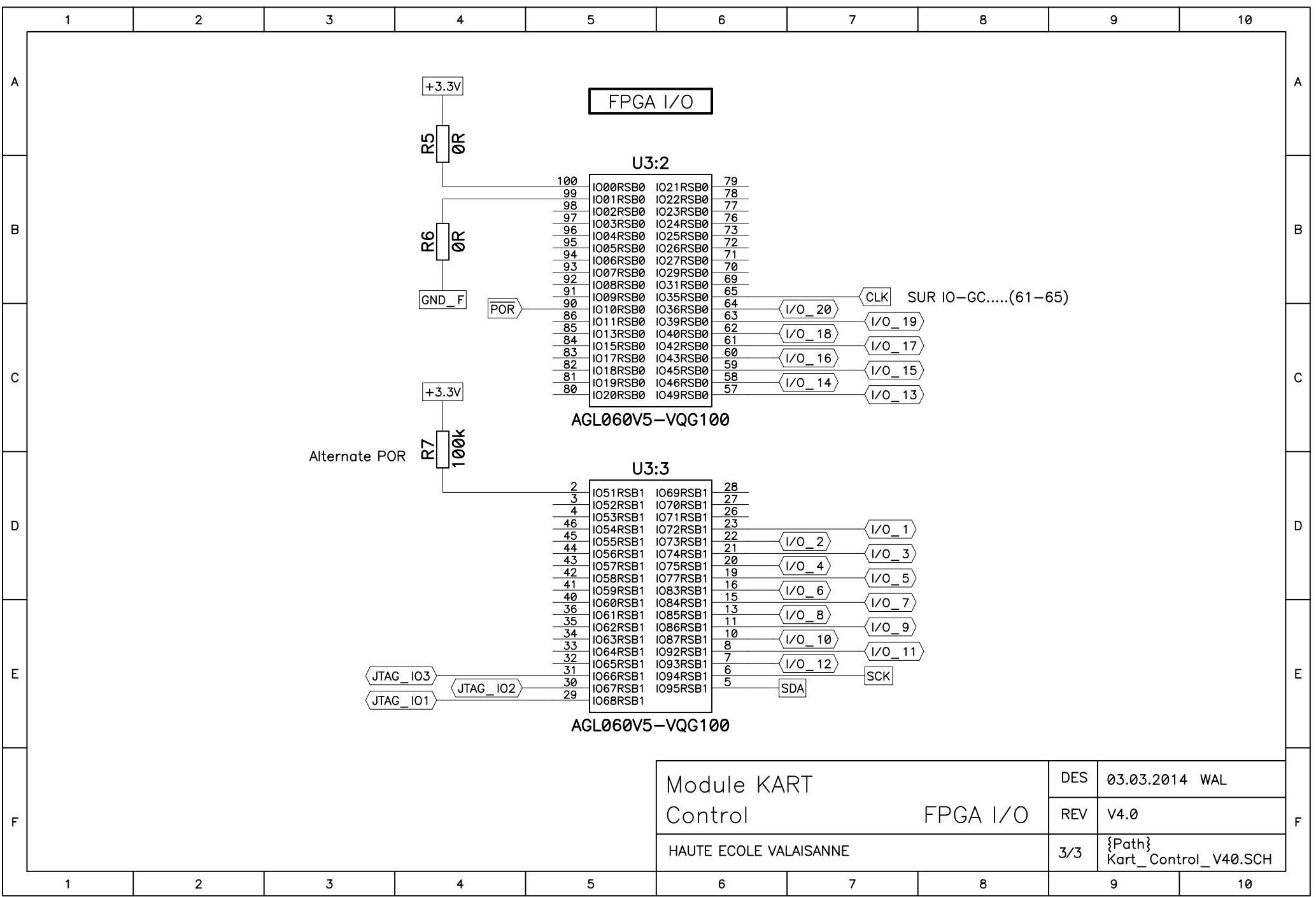
POWER 1.5V



DECOUPLING CAPACITORS



Module KART Control	DES	03.03.2014 WAL
	REV	V4.0
HAUTE ECOLE VALAISANNE	2/3	{Path} Kart_Control_V40.SCH



Module KART Control	DES	03.03.2014 WAL
	REV	V4.0
HAUTE ECOLE VALAISANNE	3/3	{Path} Kart_Control_V40.SCH

FPGA I/O