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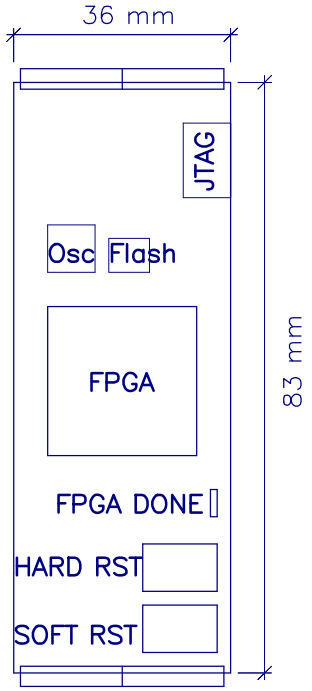
CanSat Master FPGA

Page	Title	Description
1	Cover	This first page
2	Connector	
3	FPGA	



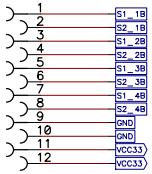
Revision	Changes
1.0	Initial Version
2.0	+ added test point for GND – removed LED on 1V2 (there exists no LED at this low voltage) + added LED on 3V3

CanSat Master FPGA cover	DES	2014–07–17 guo
	REV	V1.0
HAUTE ECOLE VALAISANNE	1/5	{Path} CanSat_ Master_ FPGA_ v2.sch

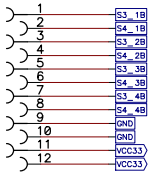
Connectors

Bottom

J1

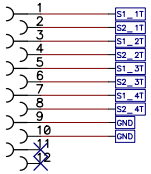


J2

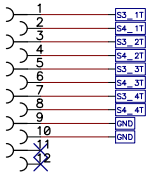


Top

J3



J4

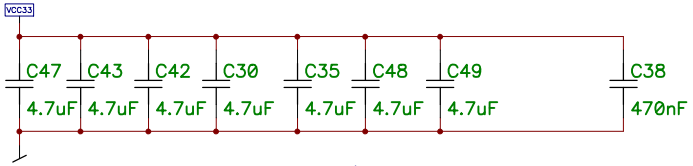


CanSat Master FPGA connector	DES	2014-07-17 guo
	REV	V1.0
HAUTE ECOLE VALAISANNE	2/5	{Path} CanSat_Master_FPGA_v2.sch

FPGA Power & Decoupling

VCCINT Decoupling

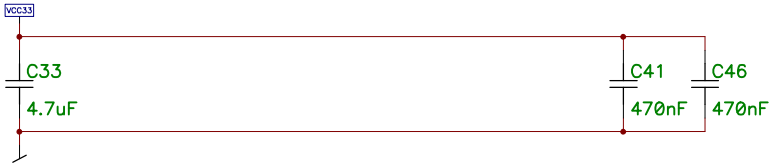
VCCAUX Decoupling



VCC0 Bank 0 Decoupling

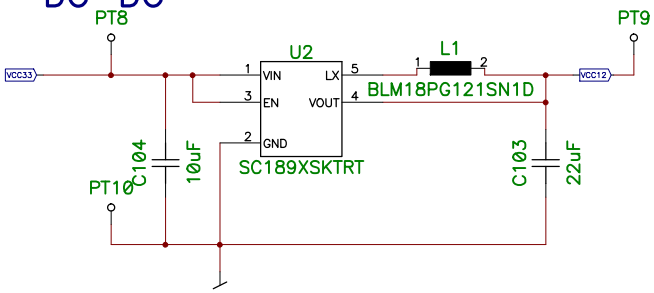
VCC0 Bank 1 Decoupling

VCC0 Bank 2 Decoupling



VCC0 Bank 3 Decoupling

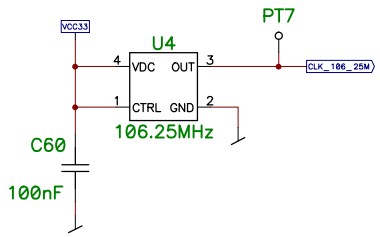
DC–DC



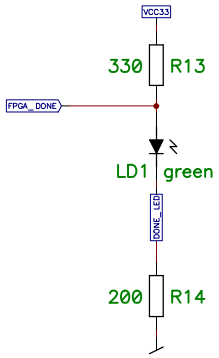
CanSat Master FPGA FPGA Power & Decoupling	DES	2014–07–17 guo
	REV	V1.0
HAUTE ECOLE VALAISANNE	3/5	{Path} CanSat_ Master_ FPGA_ v2.sch

FPGA Config

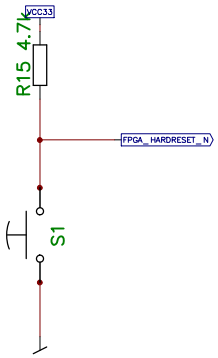
Main Oscillator



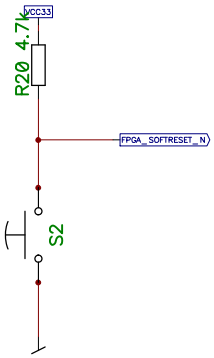
FPGA Done LED



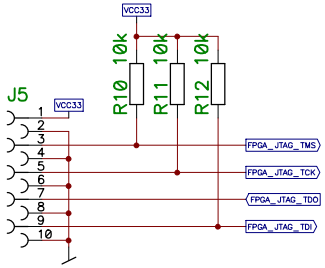
FPGA Hardreset Reprogram



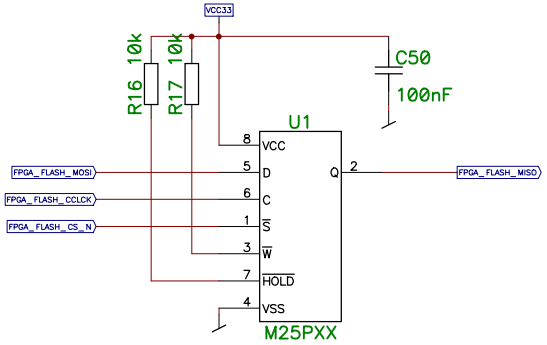
FPGA Softreset Initialize design



JTAG connector

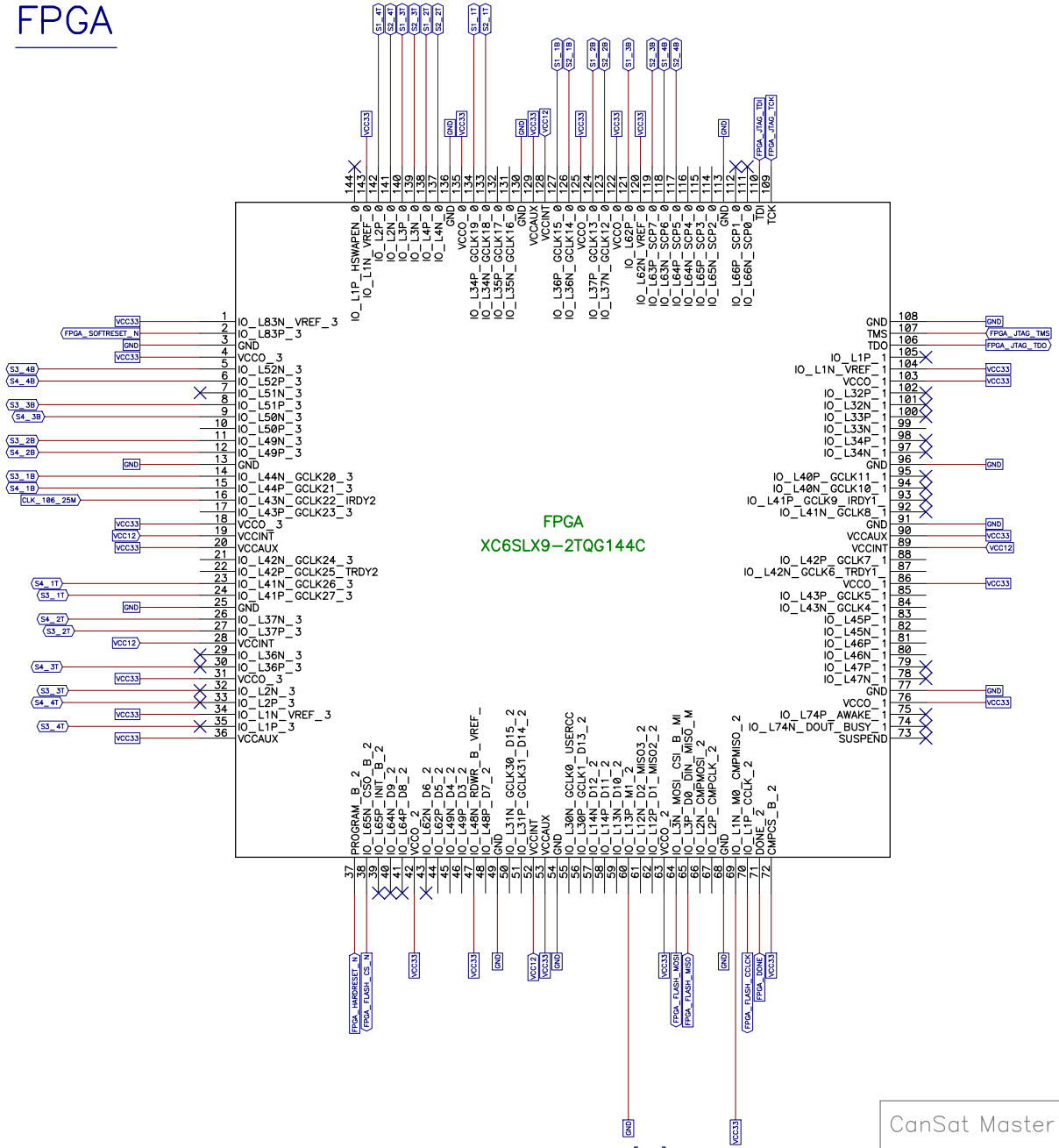


SPI Flash



CanSat Master FPGA FPGA Config	DES	2014-07-17 guo
	REV	V1.0
HAUTE ECOLE VALAISANNE	4/5	{Path} CanSat_Master_FPGA_v2.sch

FPGA



Connections Guidelines:
- CLK_106_25M has to be connected to a GLCK
- Sx_1B, Sx_1T has to be connected to a GLCK
- all Pins of the same Sx have to be on the same bank

CanSat Master FPGA	DES	2014-07-17 guo
FPGA	REV	V1.0
HAUTE ECOLE VALAISANNE	5/5	{Path} CanSat_Master_FPGA_v2.sch