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CanSat Master FPGA

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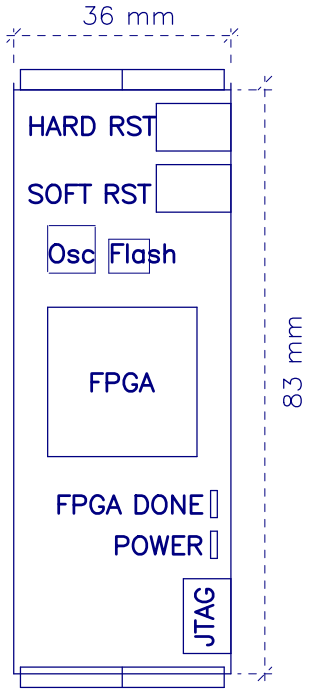


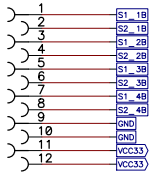
Revision	Changes
1.0	Initial Version
2.0	+ added test point for GND – removed LED on 1V2 (there exists no LED at this low voltage) + added LED on 3V3 + added possibility to pull–up/down HSWAPEN
2.1	* fixed naming of top connecotr signals (J3,J4): S1<–>S2, S3<–>S4

CanSat Master FPGA cover	DES	2014–07–17 guo
	REV	V1.0
HAUTE ECOLE VALAISANNE	1/5	{Path} CanSat_Master_FPGA_v2–1.sch

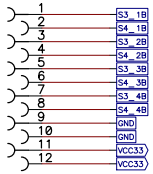
Connectors

Bottom

J1

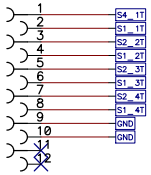


J2

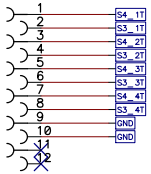


Top

J3



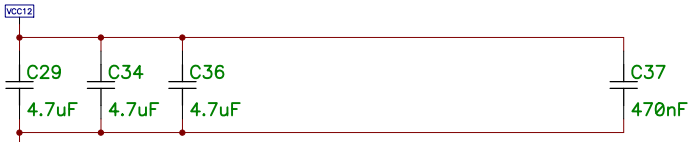
J4



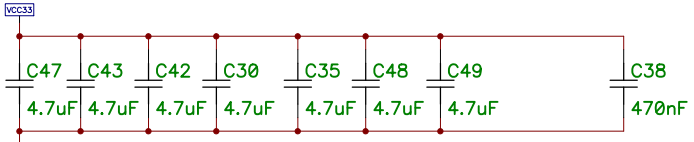
CanSat Master FPGA connector	DES	2014-07-17 guo
	REV	V1.0
HAUTE ECOLE VALAISANNE	2/5	{Path} CanSat_Master_FPGA_v2-1.sch

FPGA Power & Decoupling

VCCINT Decoupling



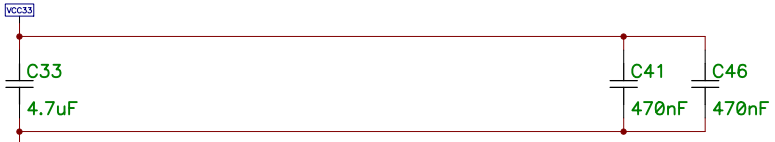
VCCAUX Decoupling



VCC0 Bank 0 Decoupling

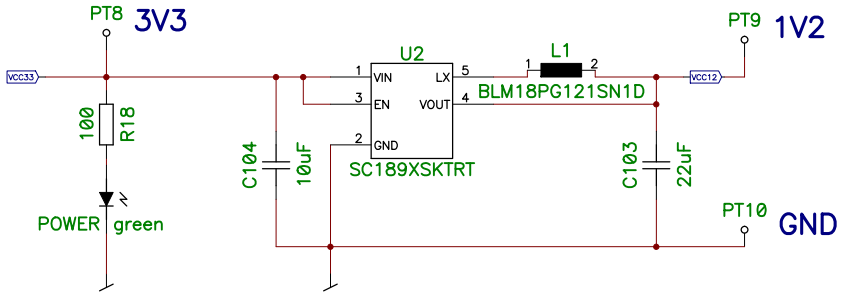
VCC0 Bank 1 Decoupling

VCC0 Bank 2 Decoupling



VCC0 Bank 3 Decoupling

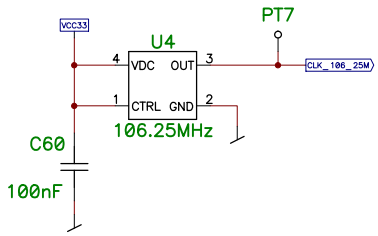
DC–DC



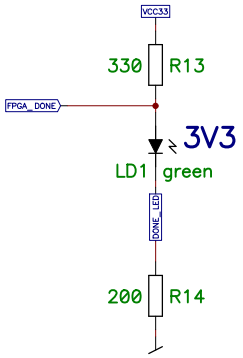
CanSat Master FPGA FPGA Power & Decoupling	DES	2014-07-17 guo
	REV	V1.0
HAUTE ECOLE VALAISANNE	3/5	{Path} CanSat_Master_FPGA_v2-1.sch

FPGA Config

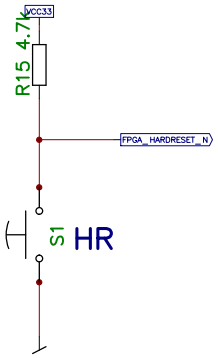
Main Oscillator



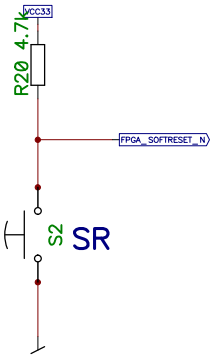
FPGA Done LED



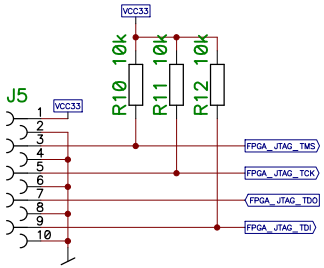
FPGA Hardreset Reprogram



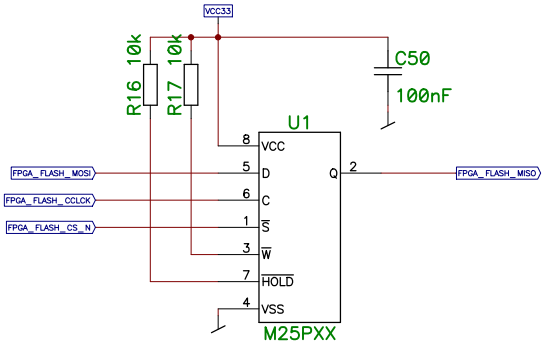
FPGA Softreset Initialize design



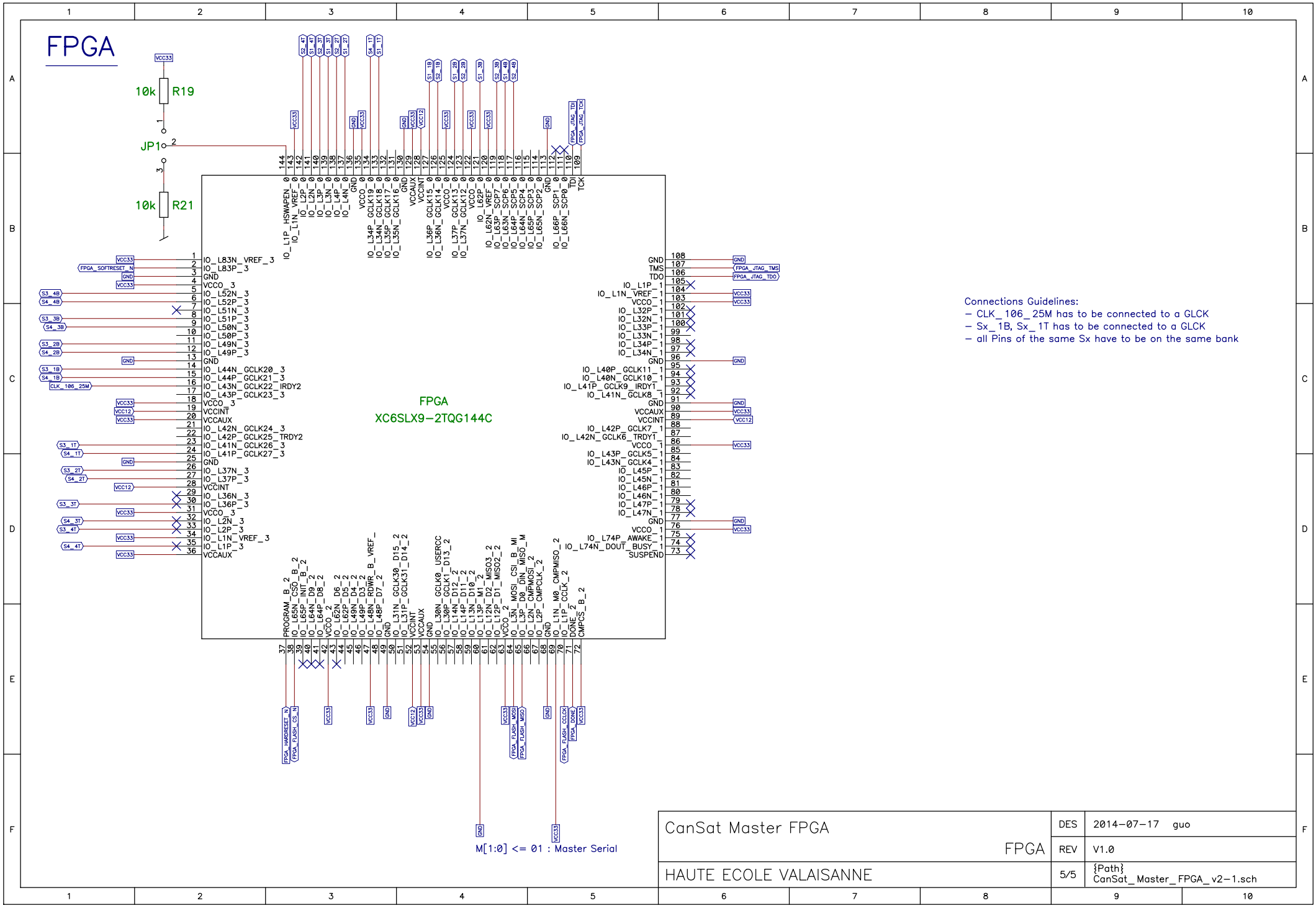
JTAG connector



SPI Flash



CanSat Master FPGA		DES	2014-07-17 guo
	FPGA Config	REV	V1.0
HAUTE ECOLE VALAISANNE		4/5	{Path} CanSat_Master_FPGA_v2-1.sch


FPGA
10k R19
JP1
10k R21
FPGA
XC6SLX9-2TQG144C
Connections Guidelines:
– CLK_106_25M has to be connected to a GLCK
– Sx_1B, Sx_1T has to be connected to a GLCK
– all Pins of the same Sx have to be on the same bank
M[1:0] <= 01 : Master Serial
CanSat Master FPGA
FPGA
HAUTE ECOLE VALAISANNE
DES 2014-07-17 guo
REV V1.0
5/5 {Path} CanSat_Master_FPGA_v2-1.sch