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Ethernettap Board : Active Ethernet Tap and Debug Board for FPGA–EBS & FPGA–RACK

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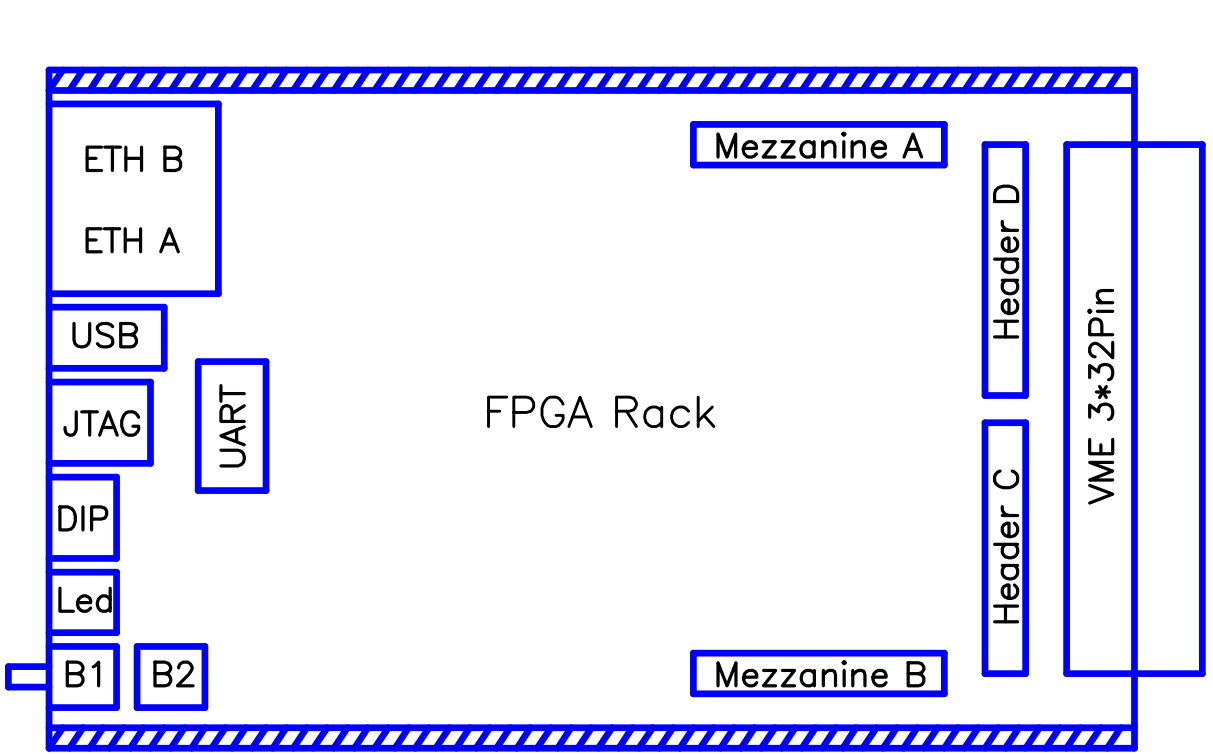
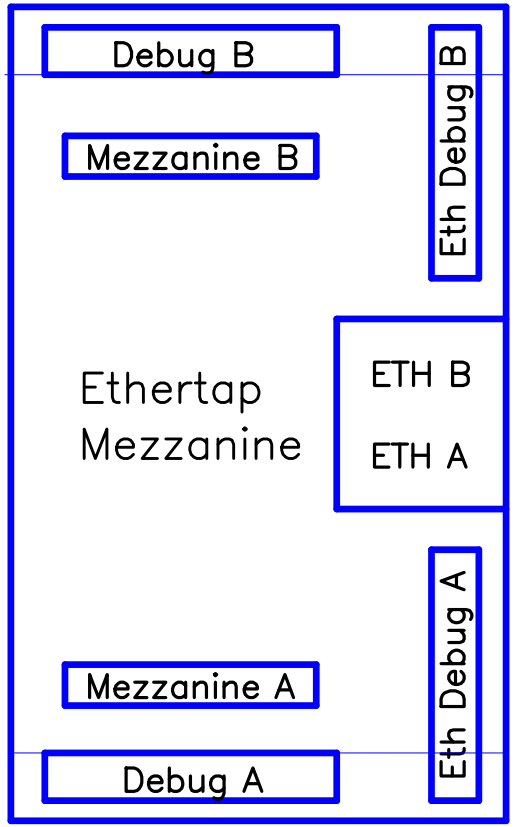
Ethernettab Board Overview

Tab overview in comparison to FPGA Rack





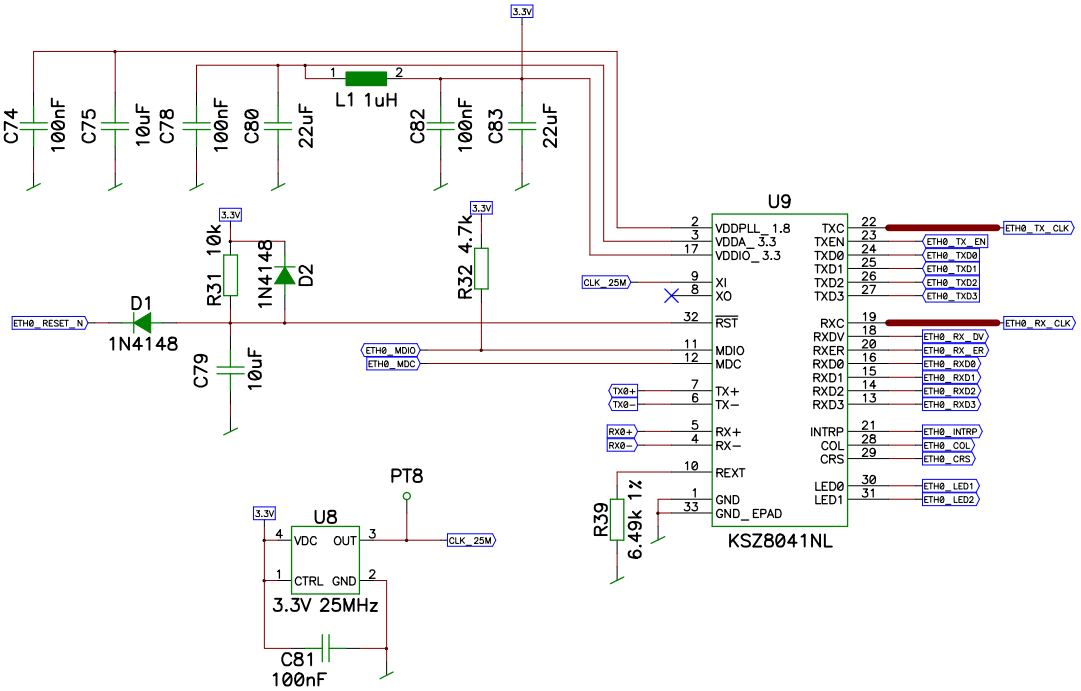
Ethernet Tap HES–SO // Valais Wallis Board		DES	{Date} zas
		REV	V1.0
HAUTE ECOLE VALAISANNE		2/9	{Path} Ethernettap_V1_0.sch

Ethernet 1

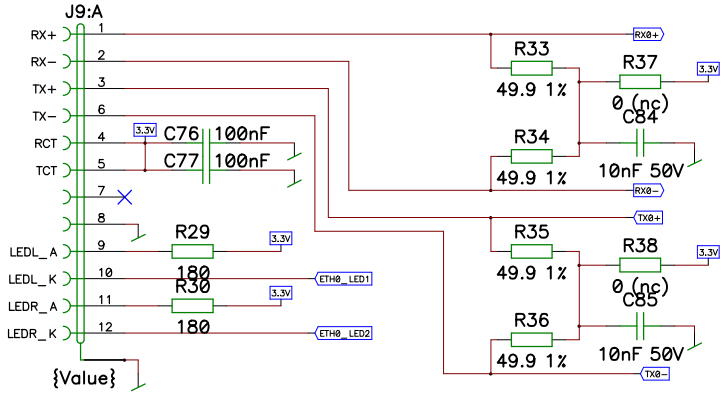
Ethernet controller 1

TX_CLK and RX_CLK must be longer than other signals on MII.

Decoupling close to VDD Pins



Ethernet connector 1

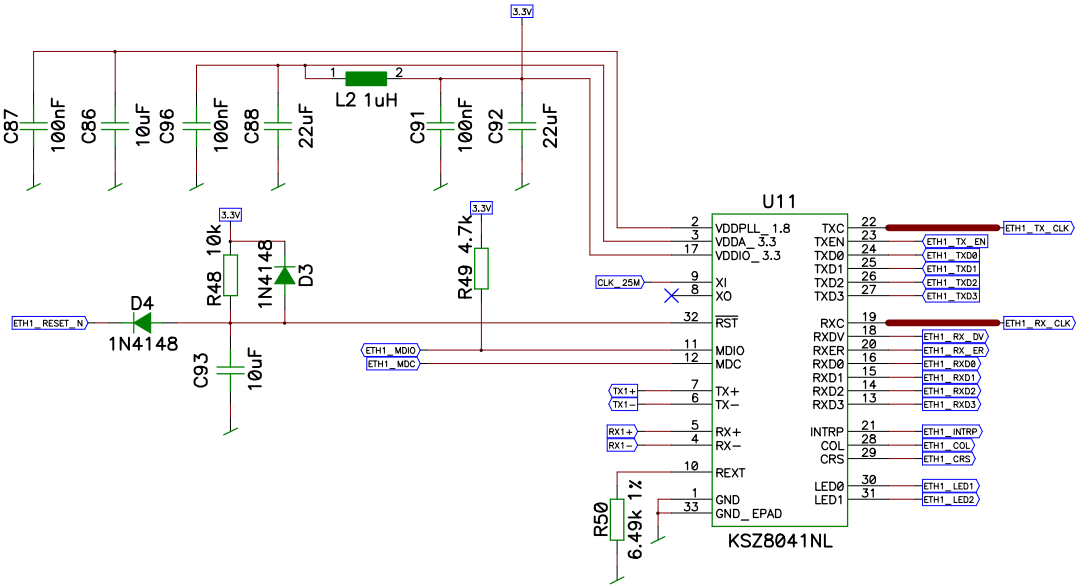


Ethernet Tap HES−SO // Valais Wallis Ethernet1 HAUTE ECOLE VALAISANNE		DES	{Date} zas
		REV	V1.0
		3/9	{Path} Ethernettap_V1_0.sch

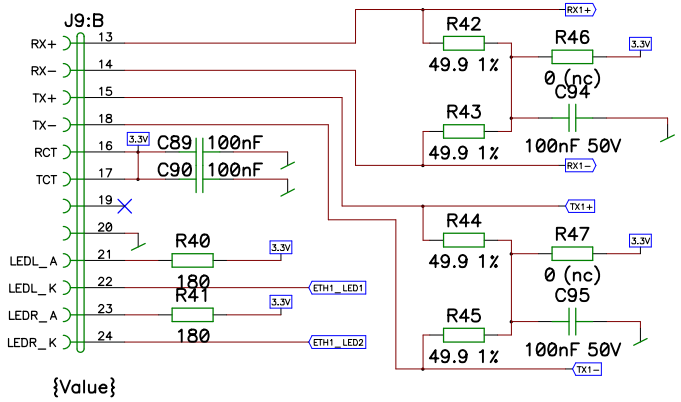
Ethernet 2

Ethernet controller 2

TX_CLK and RX_CLK must be longer
than other signals on MII.
Decoupling close to VDD Pins



Ethernet connector 2

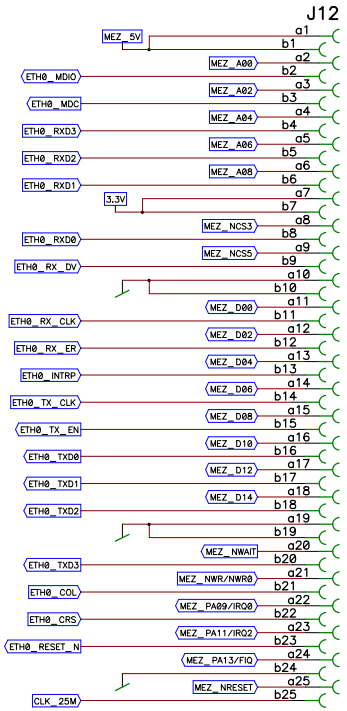


Ethernet Tap HES−SO // Valais Wallis Ethernet2		DES	{Date} zas
		REV	V1.0
HAUTE ECOLE VALAISANNE		4/9	{Path} Ethernettap_V1_0.sch

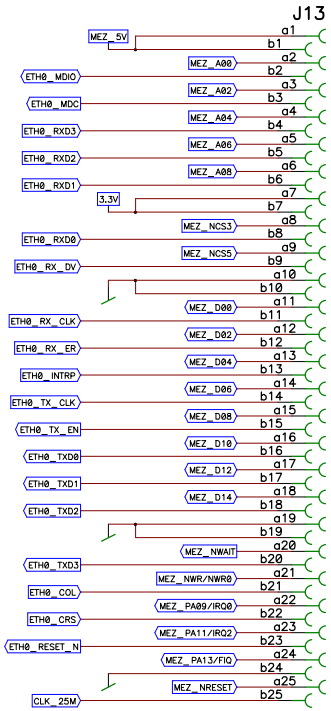
Mezzanine

Mezza A

TOP SIDE

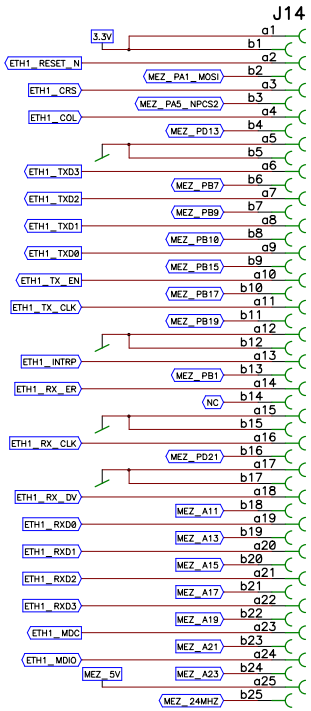


BOTTOM SIDE

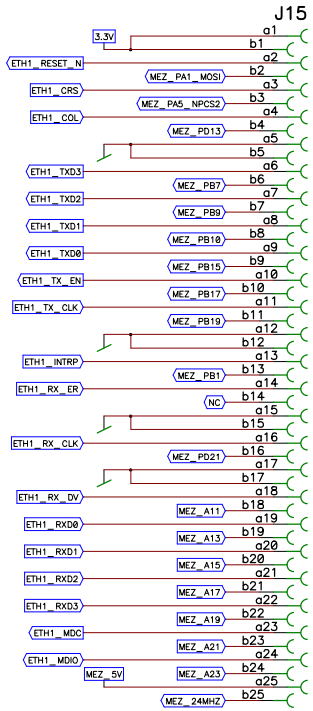


Mezza B

TOP SIDE



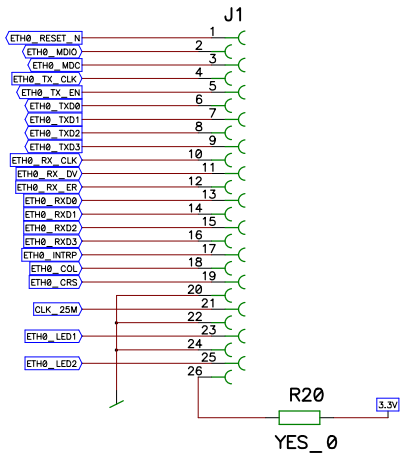
BOTTOM SIDE



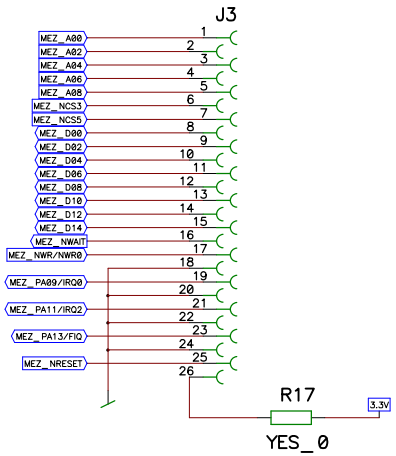
Ethernet Tap HES–SO // Valais Wallis Mezzanine	DES	{Date} zas
	REV	V1.0
HAUTE ECOLE VALAISANNE	5/9	{Path} Ethernettap_V1_0.sch

Debug

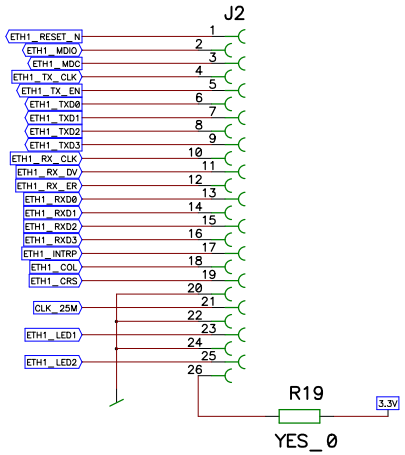
ETH Debug A



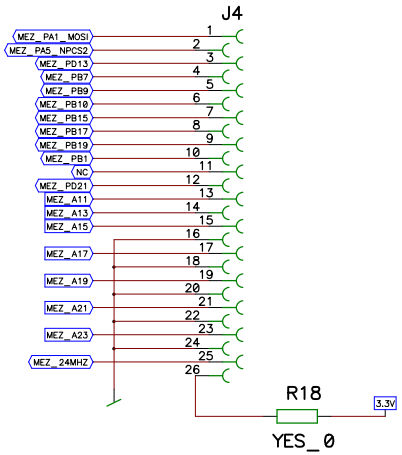
Debug A

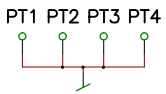


ETH Debug B



Debug B





Ethernet Tap HES–SO // Valais Wallis — Debug HAUTE ECOLE VALAISANNE	DES	{Date} zas
	REV	V1.0
	6/9	{Path} Ethernettap_V1_0.sch