

HES-SO Valais Wallis
 Route du Rawyl 47
 1950 Sion 2
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Dormouse

FPGA_Rack_4ethernet

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FPGA Rack 4ethernet
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Cover

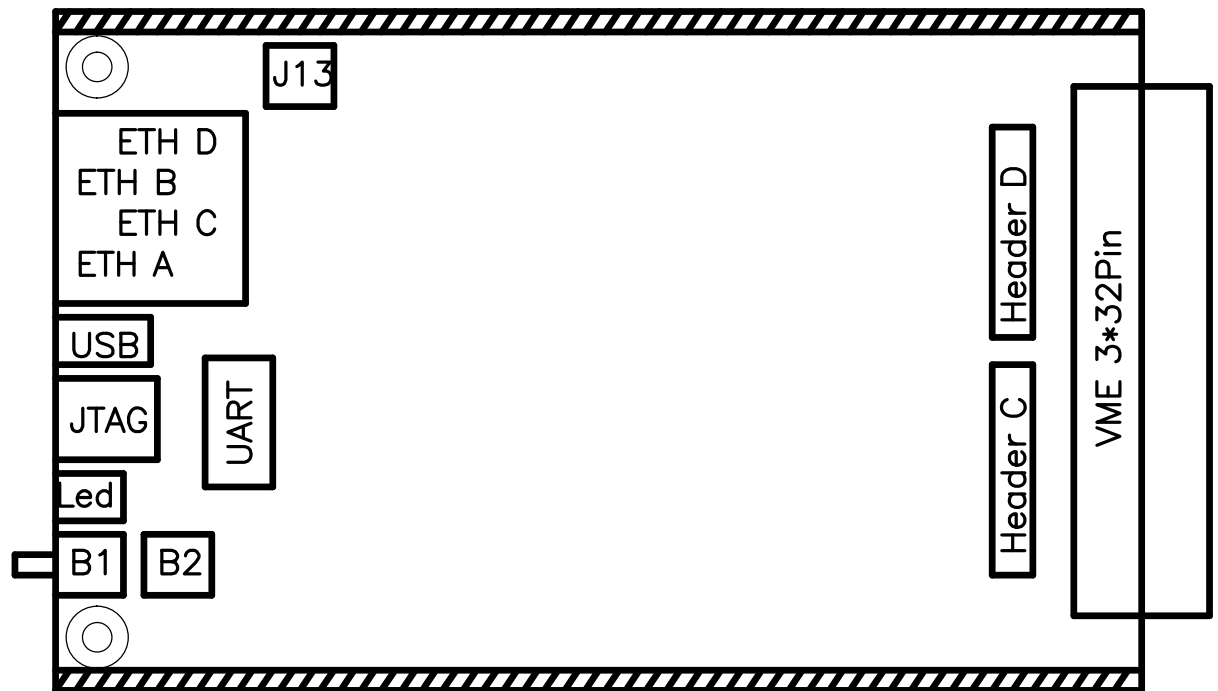
DES	{Date}	guo
REV	v1.0	
1/24	{Path}	FPGA_Rack_4ethernet_v1.sch

Brief revision history

Revision	Major changes
1.0	Based on FPGA_Rack_v1_0 – removed mezz connectors * changed Ethernet connector to 2x2 + added PHY for each Ethernet connection (removed PTP PHY) * changed USB connector from mini to micro

Build instructions

- * CLK_25M should have the same path length to all 4 Ethernet connectors
- * ETHx_TX_CLK and ETHx_RX_CLK must be longer than other signals on MII
- * holes for pcb holder distrelec 321766



[Hatched Pattern] = min. 3mm with no components for Rack insertion
 do not mount VME, Header C&D and SRRAM

FPGA Rack 4ethernet HES-SO // Valais Wallis	DES	{Date}	guo
Board	REV	v1.0	
HAUTE ECOLE VALAISANNE	2/24	{Path}	FPGA_Rack_4ethernet_v1.sch

Power supply

5V -> From VME or USB
 3.3V -> From LTM4615 (1)
 1.2V -> From LTM4615 (2)
 1.8V -> From LTM4615 LDO
 2.5V -> From LDO

Layout Hints
 - THERMAL_SW1 and THERMAL_SW2
 - Floating on separate copper planes
 - Decoupling capacitors close to pins

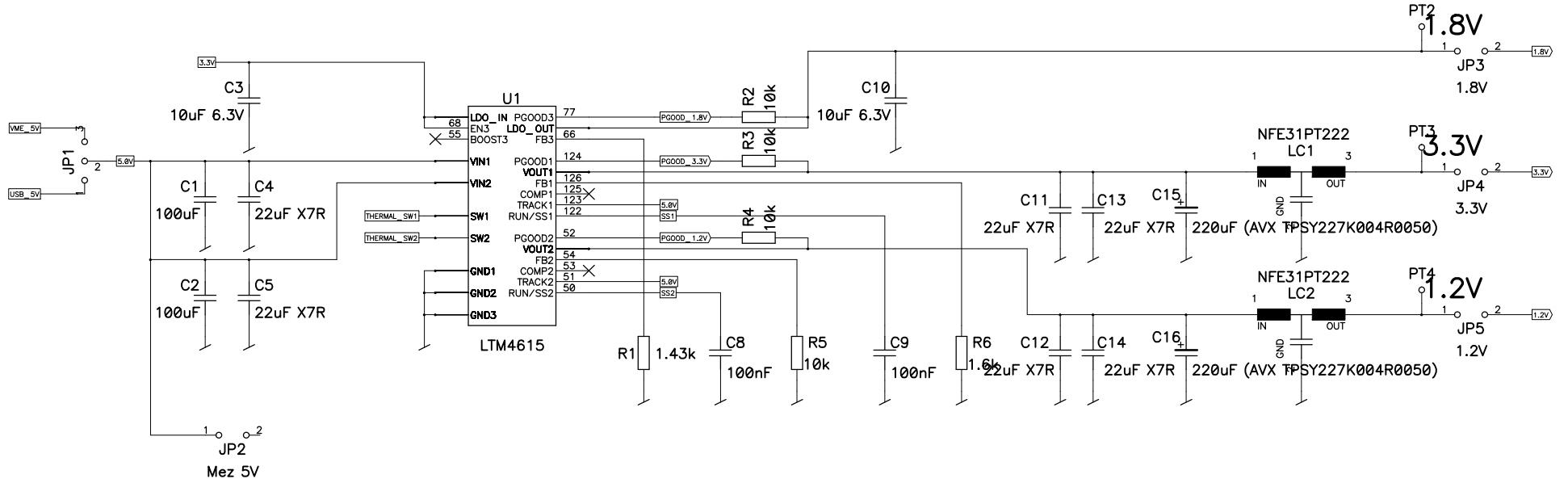
LDO VOUT
 $V_{LDO_OUT} = 0.4V * (4.99k + R_{FB_LDO}) / R_{FB_LDO}$
 $\rightarrow R_{FB_LDO} = 1.996k / (V_{LDO_OUT} - 0.4V)$
 $R_{FB_LDO} (V_{out} = 1.8V) = 1.996k / (1.8 - 0.4) = 1.42571k \rightarrow 1.43k \ 1\% \rightarrow 1.80563V$

$V_{OUT} = 0.8V * (4.99k + R_{FB}) / R_{FB}$
 $\rightarrow R_{FB} = 3.992k / (V_{out} - 0.8)$

$R_{FB} (V_{out} = 3.3V) = 3.992k / (3.3 - 0.8) = 1.5968k \rightarrow 1.6k \ 1\% \rightarrow 3.295V$

$R_{FB} (V_{out} = 1.2V) = 3.992k / (1.2 - 0.8) = 9.98k \rightarrow 10k \ 1\% \rightarrow 1.1992V$

3.3V @ 4A / 1.2V @ 4A / 1.8V @ 1.5A



2.5V @ 950mA



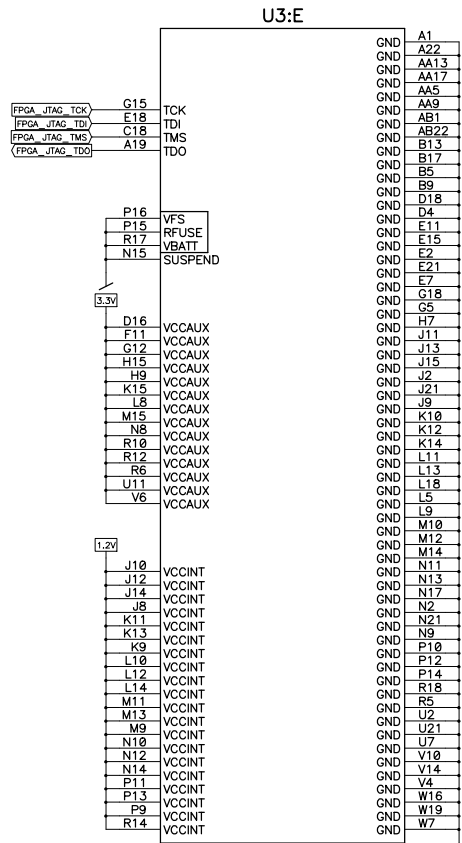
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Power

DES	{Date}	guo
REV	v1.0	
3/24	{Path}	FPGA_Rack_4ethernet_v1.sch

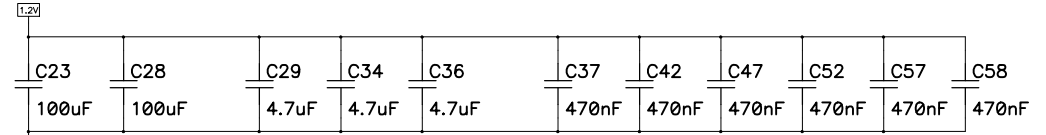
FPGA Power

Pins NOT AVAILABLE ON LX45
 ONLY AVAILABLE ON LX100 / 150
 - VFS
 - RFUSE
 - VBATT

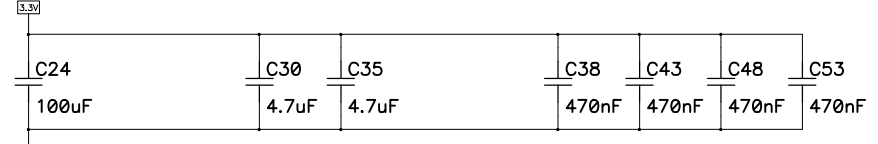


FPGA Decoupling

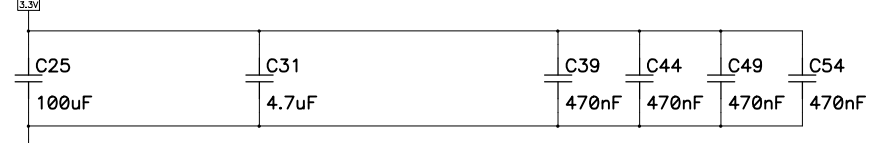
VCCINT Decoupling
 LX45 -> 1x100uF / 1x4.7uF / 2x0.47uF
 LX100 -> 1x100uF / 2x4.7uF / 4x0.47uF
 LX150 -> 2x100uF / 3x4.7uF / 6x0.47uF



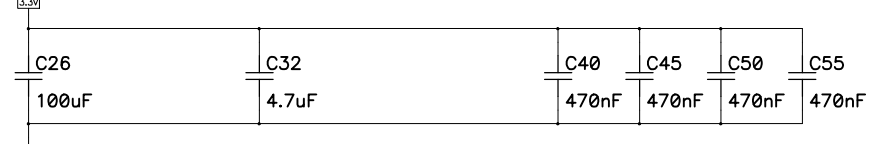
VCCAUX Decoupling
 LX45, LX100, LX150 -> 1x100uF / 2x4.7uF / 4x0.47uF



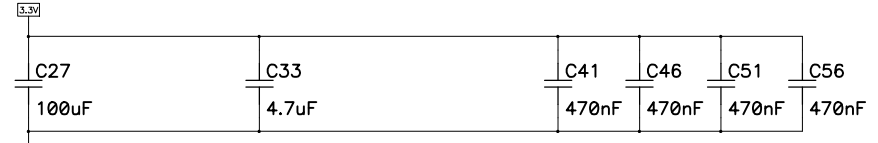
VCC0 Bank 0 Decoupling
 LX45, LX100, LX150 -> 1x100uF / 1x4.7uF / 2x0.47uF



VCC0 Bank 1 Decoupling
 LX45, LX100, LX150 -> 1x100uF / 1x4.7uF / 3x0.47uF



VCC0 Bank 2 Decoupling
 LX45 -> 1x100uF / 1x4.7uF / 4x0.47uF
 LX100, LX150 -> 1x100uF / 1x4.7uF / 3x0.47uF



VCC0 Bank 3 Decoupling
 LX45, LX100, LX150 -> 1x100uF / 1x4.7uF / 3x0.47uF



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FPGA Power

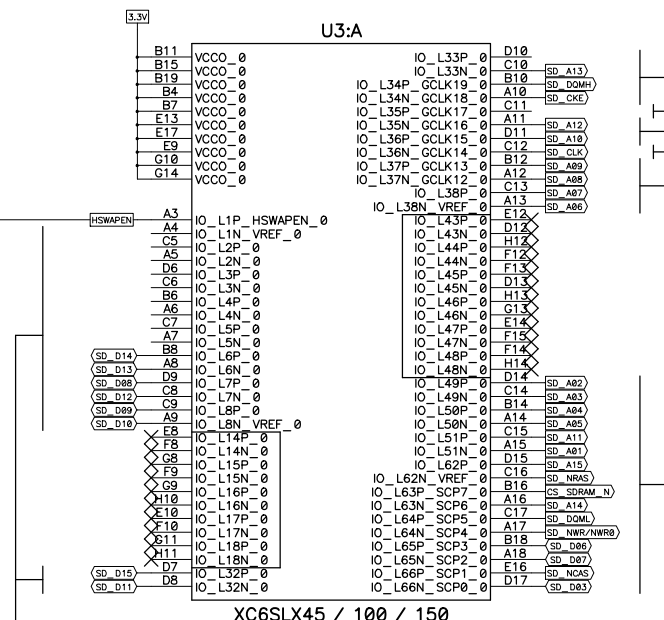
DES	{Date}	guo
REV	v1.0	
4/24	{Path}	FPGA_Rack_4ethernet_v1.sch

FPGA Bank 0 & 2

Pins NOT AVAILABLE ON LX45
 ONLY AVAILABLE ON LX100 / 150
 - IO_L14P_0, IO_L14N_0, IO_L15P_0,
 IO_L15N_0, IO_L16P_0, IO_L16N_0,
 IO_L17P_0, IO_L17N_0, IO_L18P_0

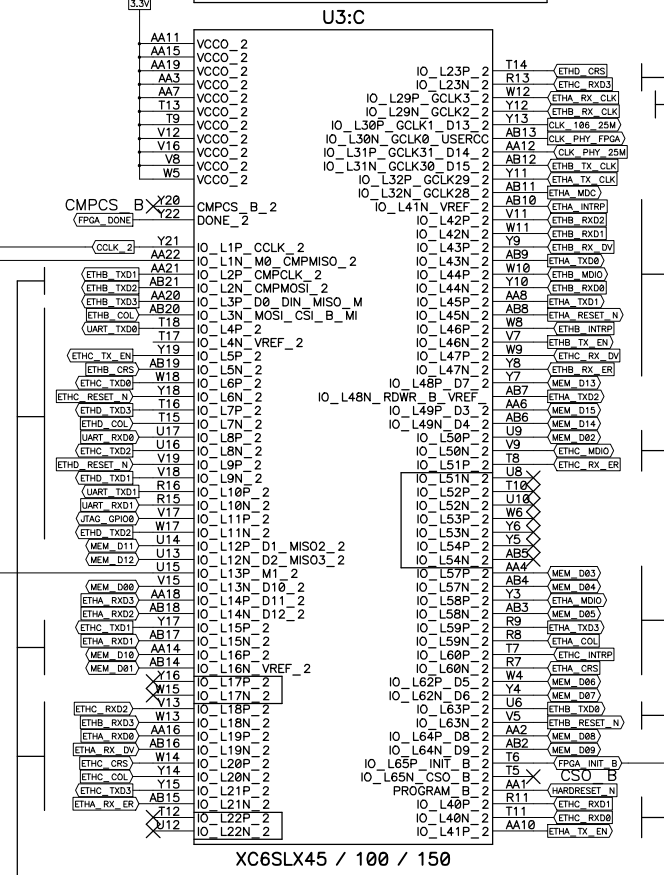
BPI Programming mode
 M0 = 0
 M1 = 0

Pins NOT AVAILABLE ON LX100
 ONLY AVAILABLE ON LX45 / 150
 - IO_L17P_2, IO_L17N_2
 - IO_L22P_2, IO_L22N_2
 - IO_L51P_2, IO_L51N_2, IO_L52P_2,
 IO_L52N_2, IO_L53P_2, IO_L53N_2,
 IO_L54P_2, IO_L54N_2

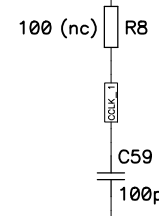


Freely moved
 within GCLK

Freely moved
 within GCLK



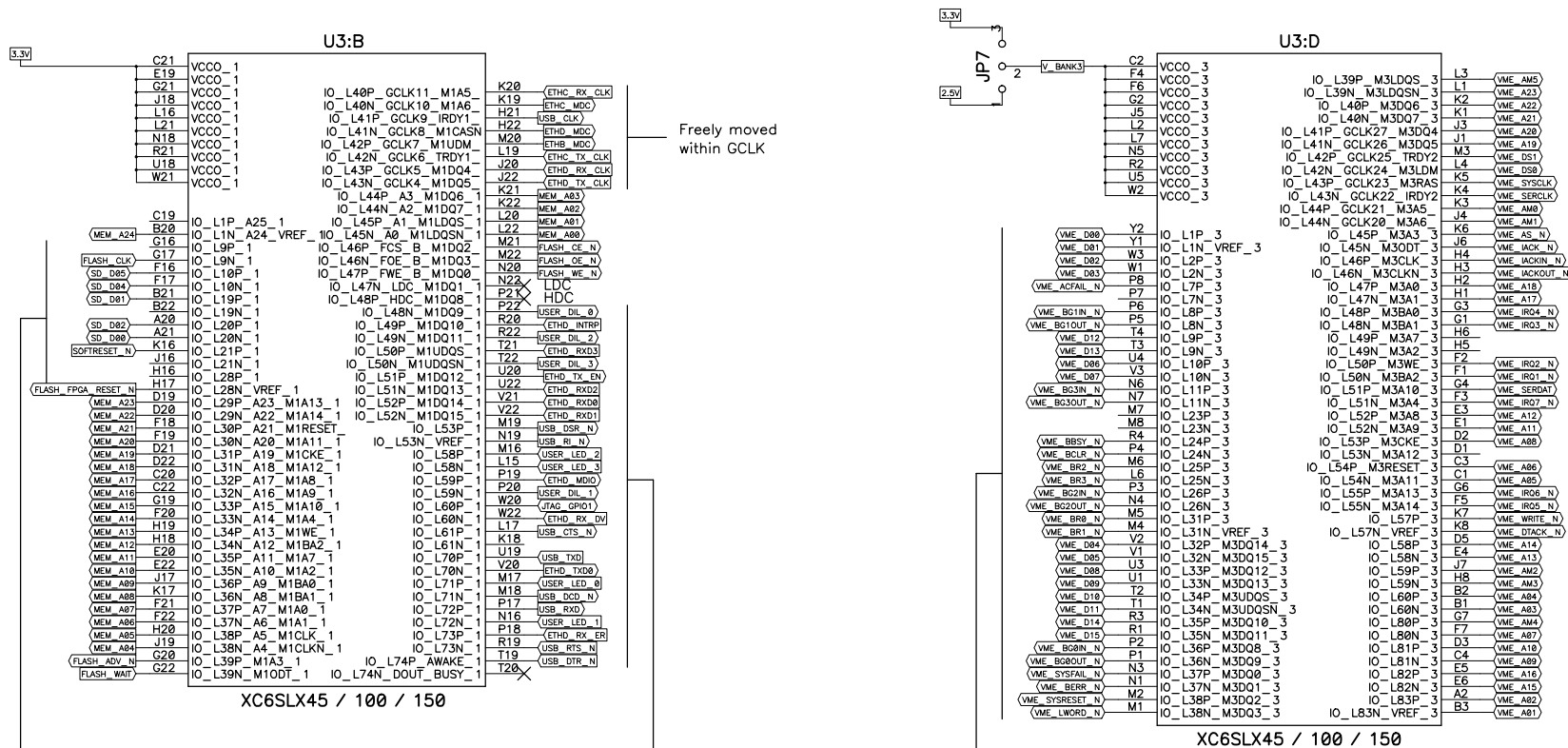
Freely moved
 within GCLK



Freely moved
 within Bank 0 & 1 & 2

FPGA Rack 4ethernet	DES	{Date}	guo
HES-SO // Valais Wallis	REV	v1.0	FPGA 1
HAUTE ECOLE VALAISANNE	5/24	{Path}	FPGA_Rack_4ethernet_v1.sch

FPGA Bank 1 & 3



Freely moved within Bank 0 & 1 & 2

Freely moved within Bank 3
But try to keep Differential Pairs together on connector

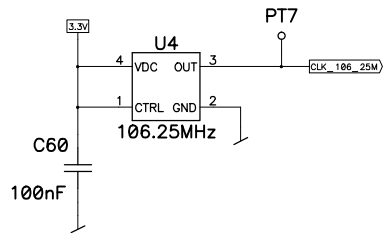
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FPGA 2

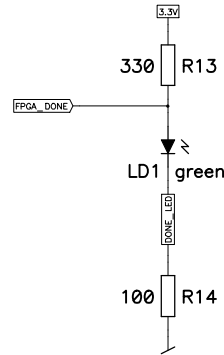
DES	{Date}	guo
REV	v1.0	
6/24	{Path}	FPGA_Rack_4ethernet_v1.sch

FPGA Config

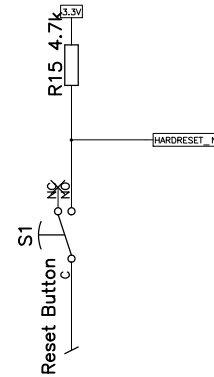
Main Oscillator



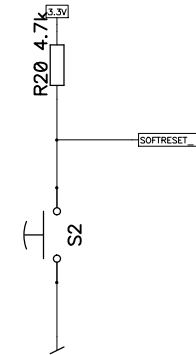
FPGA Done LED



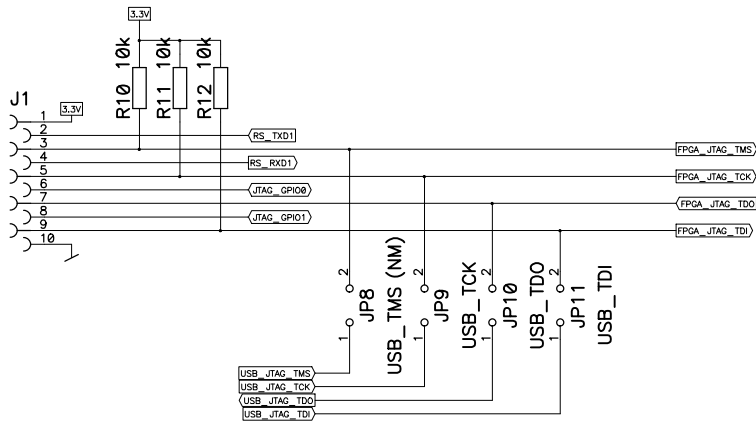
FPGA Hardreset Reprogram



FPGA Softreset

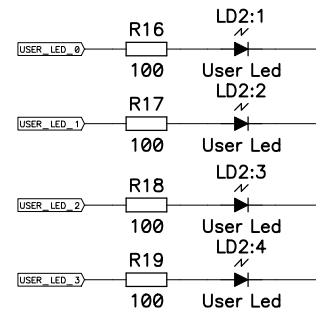


JTAG connector

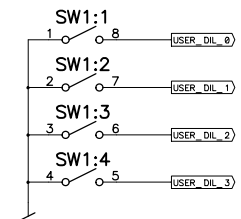


USER LED's

$$R = (3.3V - 2V) / 20mA = 65$$



USER DIP Switches



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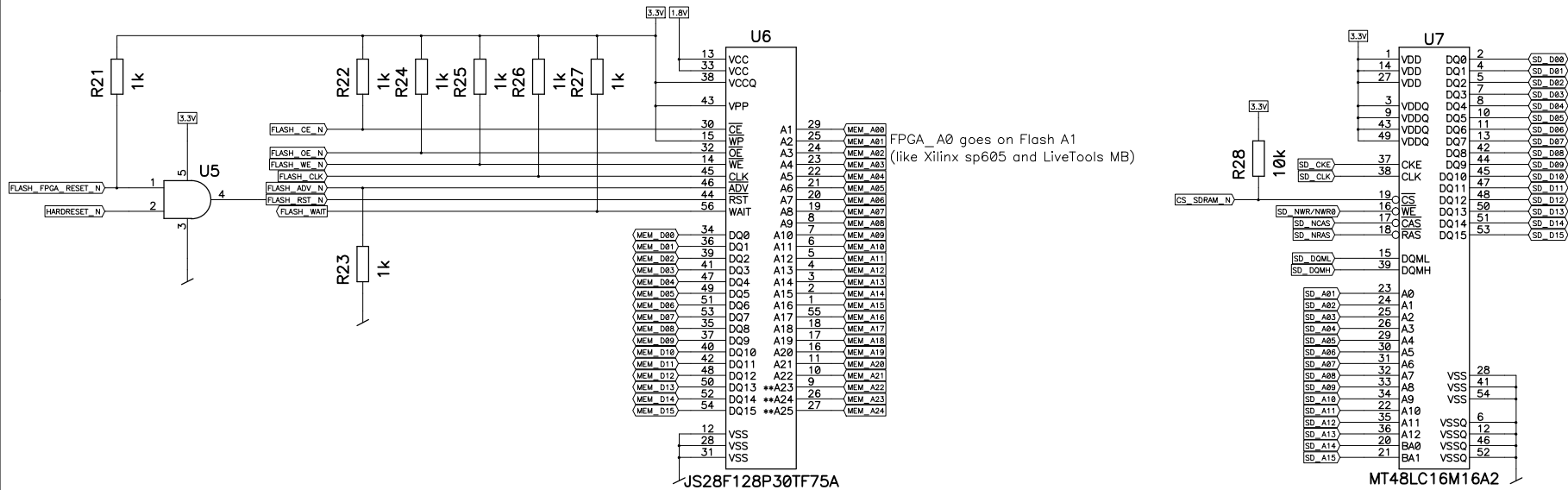
FPGA Config

DES	{Date}	guo
REV	v1.0	
7/24	{Path}	FPGA_Rack_4ethernet_v1.sch

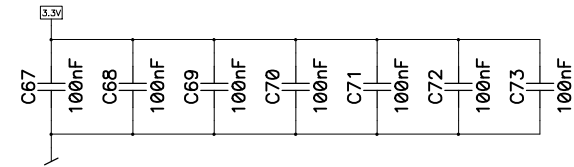
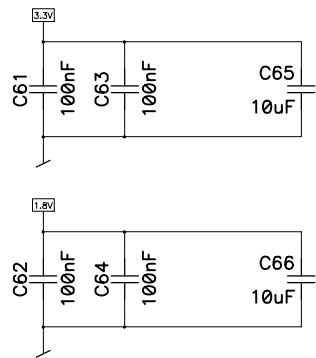
Memory Flash RAM

Flash

SDRAM



FPGA_A0 goes on Flash A1
(like Xilinx sp605 and LiveTools MB)

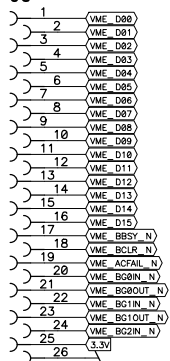


FPGA Rack 4ethernet HES-SO // Valais Wallis HAUTE ECOLE VALAISANNE	DES	{Date}	guo
	REV	v1.0	Memory
	8/24	{Path}	FPGA_Rack_4ethernet_v1.sch

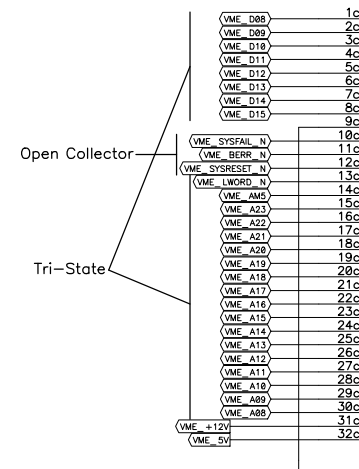
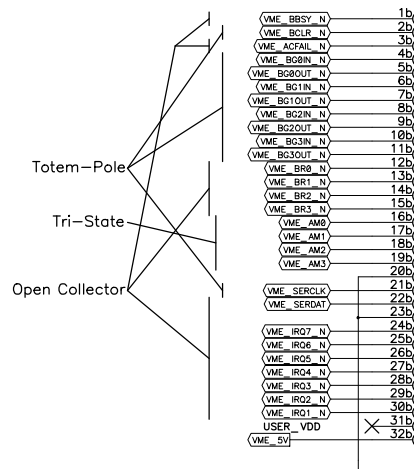
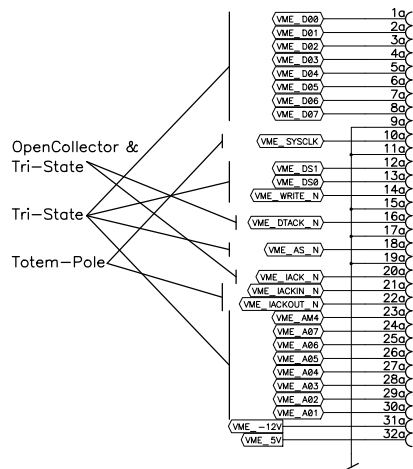
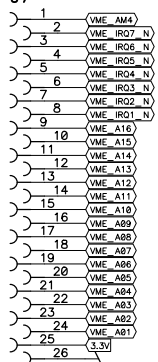
VME 96Pin

Do not mount. Will be mounted if and when needed.

J6



J7



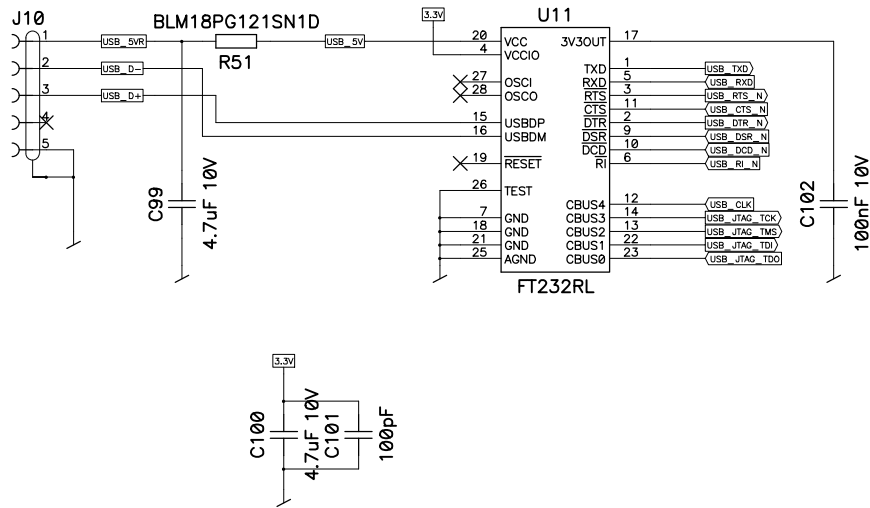
Pins on J10 and J11 can be freely moved except power

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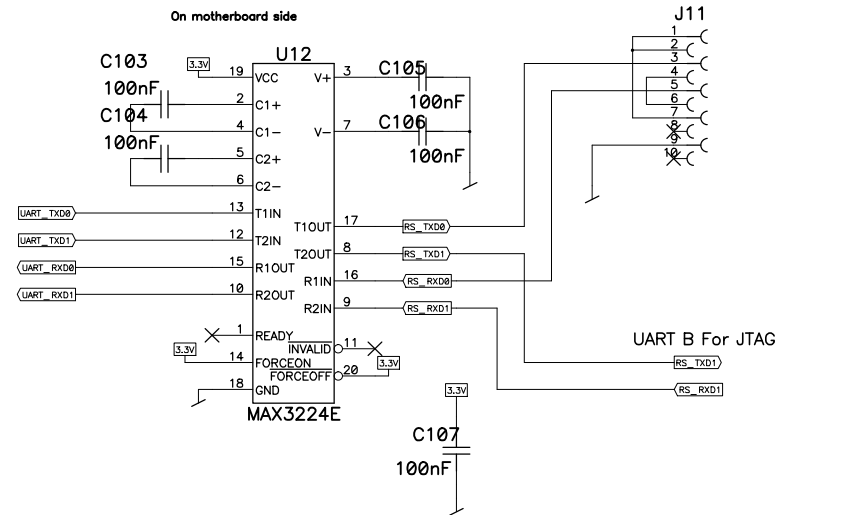
VME

DES	{Date}	guo
REV	v1.0	
9/24	{Path}	FPGA_Rack_4ethernet_v1.sch

UART & FTDI



RS 232 Serial ports



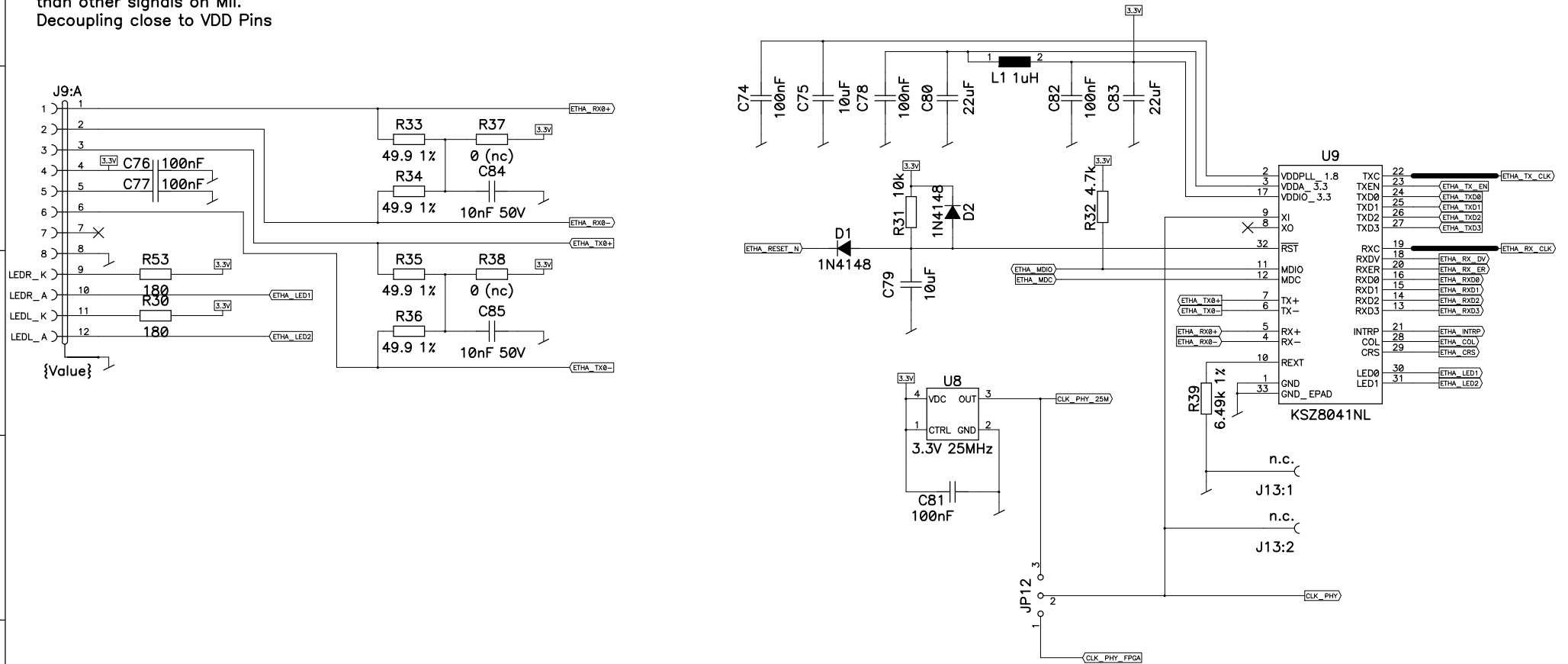
FPGA Rack 4ethernet
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UART & FTDI

DES	{Date}	guo
REV	v1.0	
10/24	{Path}	FPGA_Rack_4ethernet_v1.sch

Ethernet A

TX_CLK and RX_CLK must be longer than other signals on MII.
Decoupling close to VDD Pins



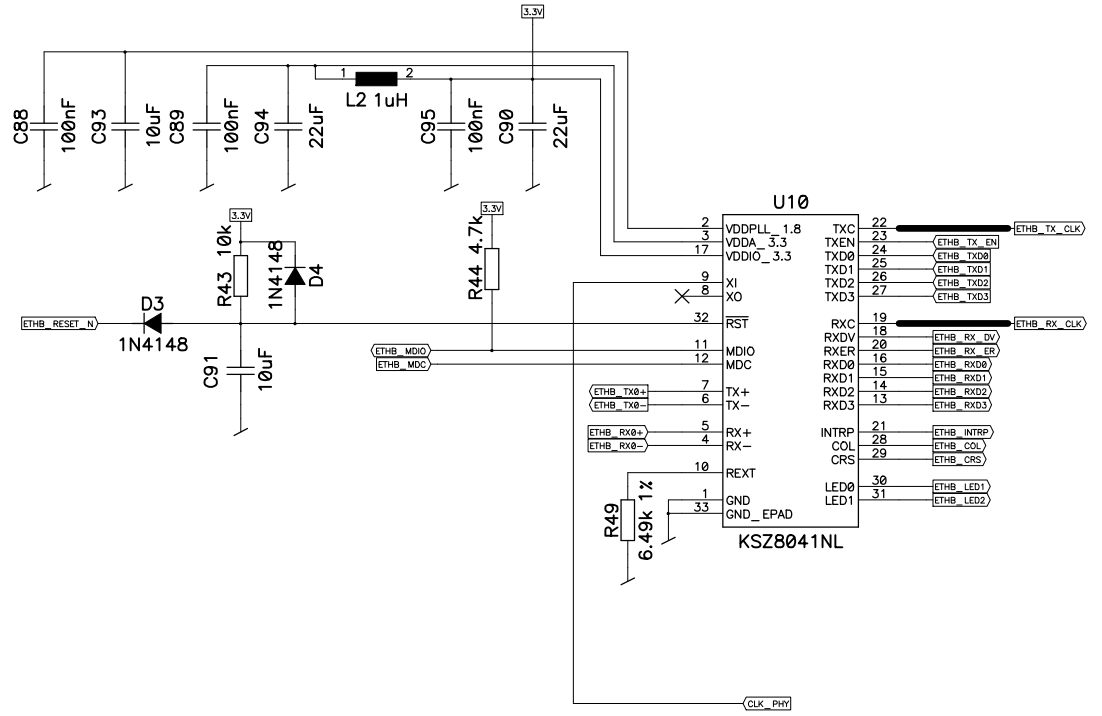
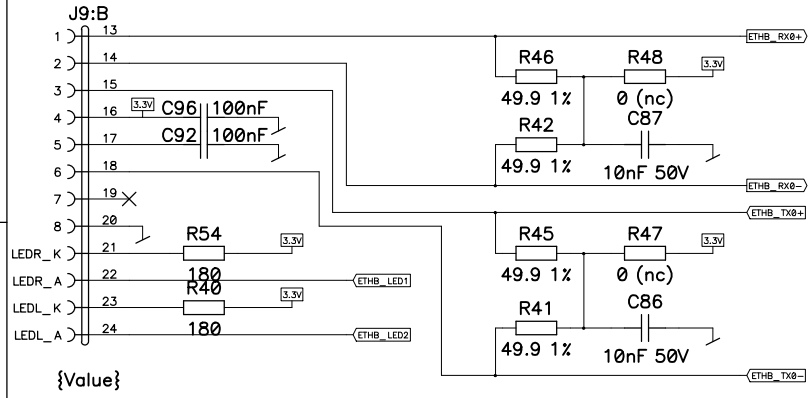
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Ethernet A

DES	{Date}	guo
REV	v1.0	
11/24	{Path}	FPGA_Rack_4ethernet_v1.sch

Ethernet B

TX_CLK and RX_CLK must be longer than other signals on MII.
Decoupling close to VDD Pins

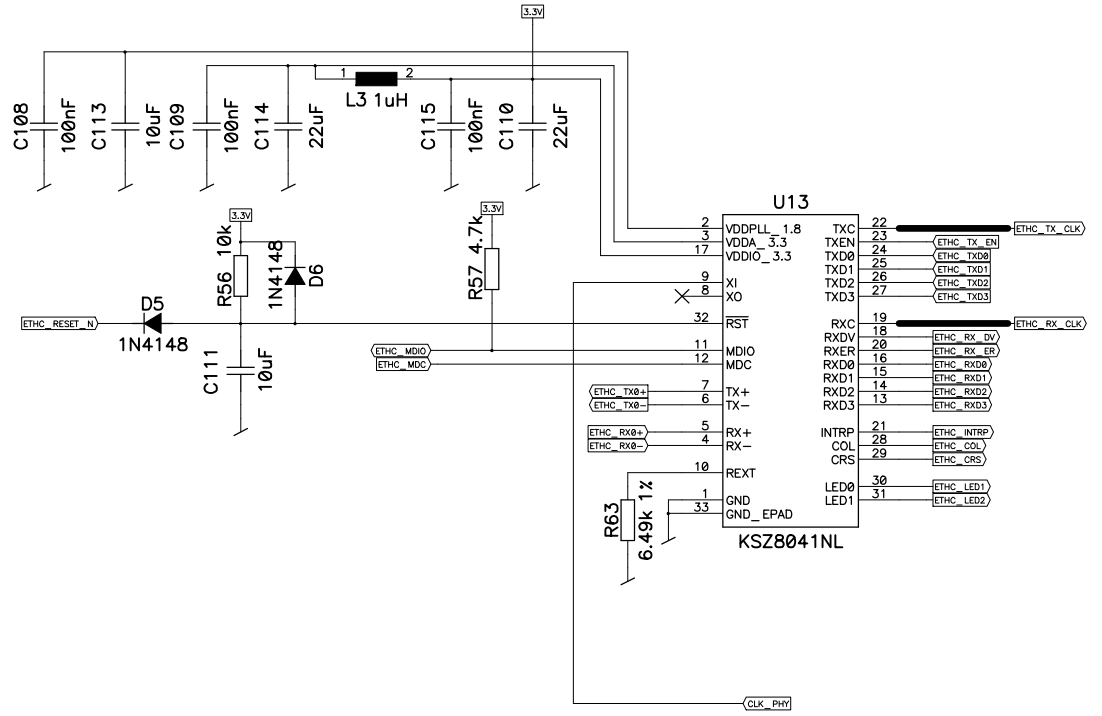
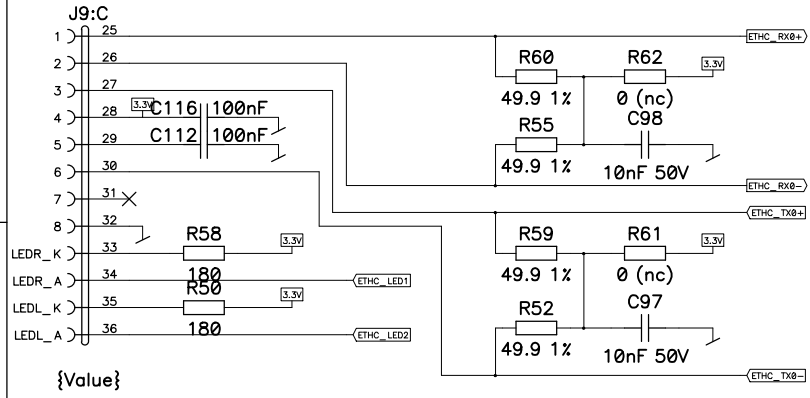


FPGA Rack 4ethernet	DES	{Date}	guo
HES-SO // Valais Wallis	REV	v1.0	
HAUTE ECOLE VALAISANNE	12/24	{Path}	FPGA_Rack_4ethernet_v1.sch

Ethernet B

Ethernet C

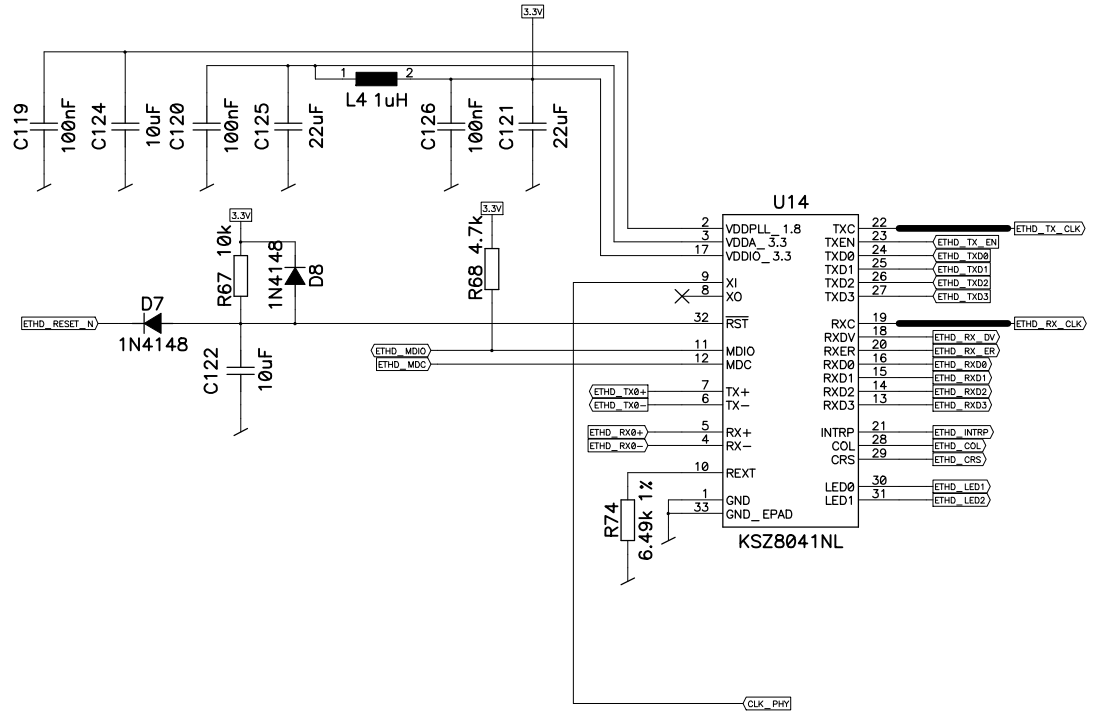
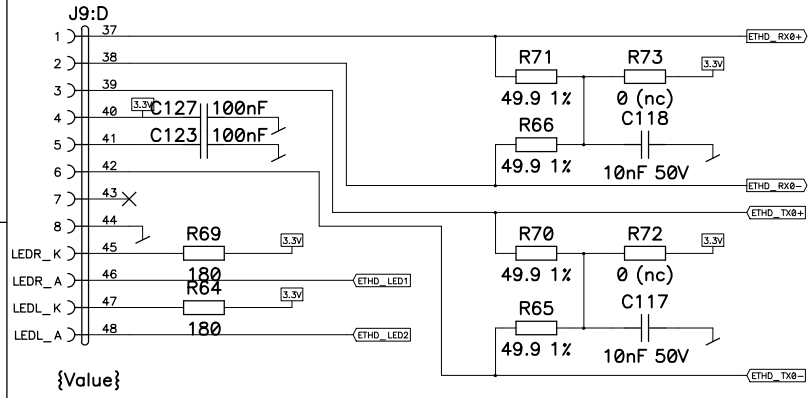
TX_CLK and RX_CLK must be longer than other signals on MII.
Decoupling close to VDD Pins



FPGA Rack 4ethernet	DES	{Date}	guo
HES-SO // Valais Wallis	REV	v1.0	Ethernet C
HAUTE ECOLE VALAISANNE	13/24	{Path}	FPGA_Rack_4ethernet_v1.sch

Ethernet D

TX_CLK and RX_CLK must be longer than other signals on MII.
Decoupling close to VDD Pins



FPGA Rack 4ethernet	DES	{Date}	guo
HES-SO // Valais Wallis	REV	v1.0	Ethernet D
HAUTE ECOLE VALAISANNE	14/24	{Path}	FPGA_Rack_4ethernet_v1.sch