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FPGA_EBS Board : Educative FPGA platform

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3	FPGA Config	Xilinx EEPROM / JTAG Connectors / FPGA Done LED / Reset Circuit
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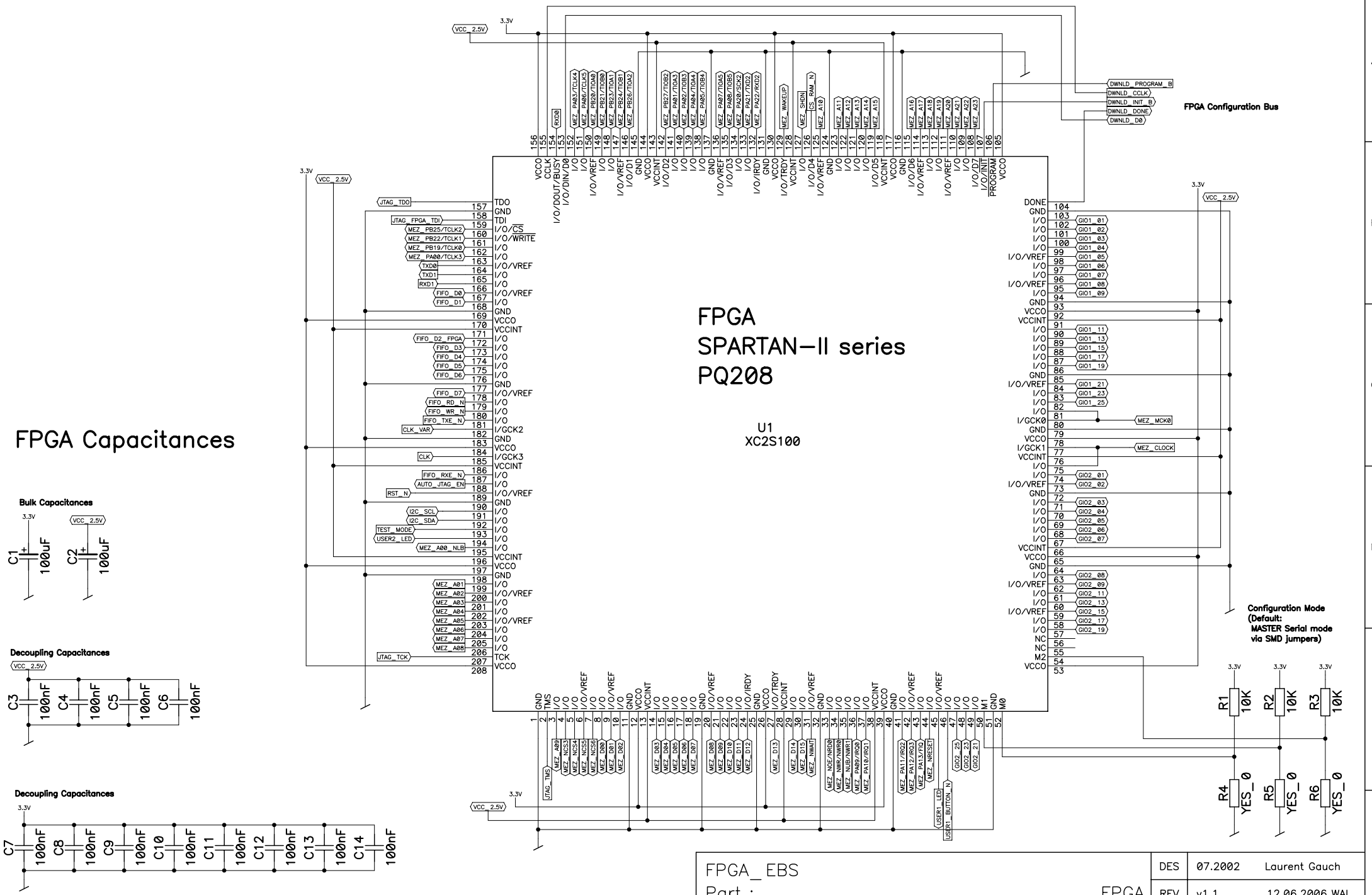
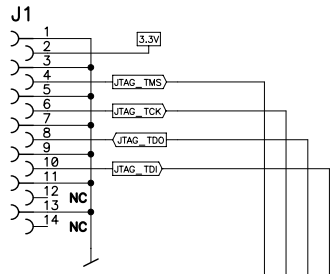
8	Power	Power Jack Connector / 3.3V ragulation / 2.5V regulation
9	USB	USB / FPGA dialog over USB / FPGA JTAG over USB

FPGA_EBS Part : Cover	DES	07.2002	Laurent Gauch
	REV	v1.1	12.06.2006 WAL
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS	1/10	...\FPGA-EBS\FPGA_EBS_V1.1 FPGA_EBS.sch	

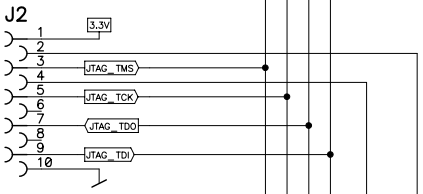

FPGA
SPARTAN–II series
PQ208
U1
XC2S100
FPGA Capacitances
Bulk Capacitances
C1 100uF
C2 100uF
Decoupling Capacitances
C3 100nF
C4 100nF
C5 100nF
C6 100nF
Decoupling Capacitances
C7 100nF
C8 100nF
C9 100nF
C10 100nF
C11 100nF
C12 100nF
C13 100nF
C14 100nF
FPGA Configuration Bus
Configuration Mode
(Default:
MASTER Serial mode
via SMD jumpers)
R1 10K
R2 10K
R3 10K
R4 YES_0
R5 YES_0
R6 YES_0
FPGA_EBS
Part : FPGA
DES 07.2002 Laurent Gauch
REV v1.1 12.06.2006 WAL
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS
2/10
...\FPGA–EBS\FPGA_EBS_V1.1
FPGA_EBS.sch

JTAG connector

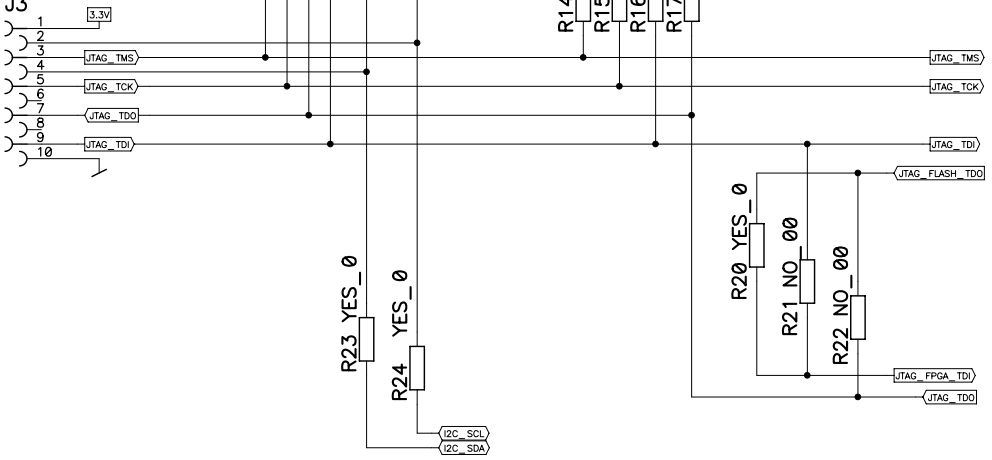
On motherboard side



On motherboard side

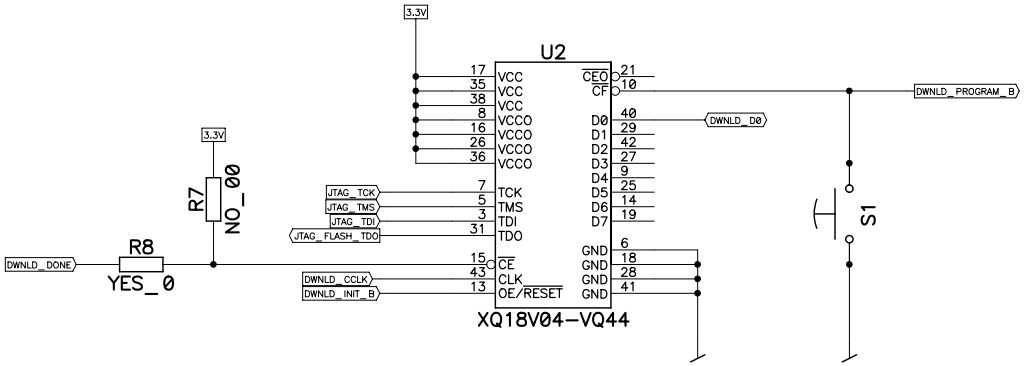


On mezzanine side



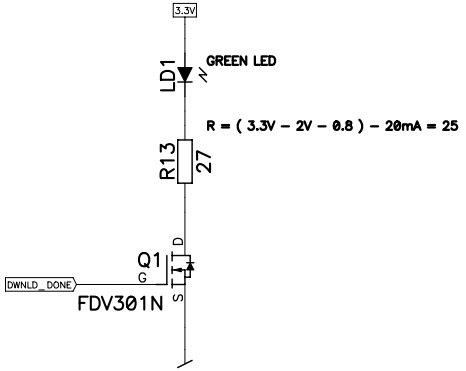
EEPROM for FPGA Configuration

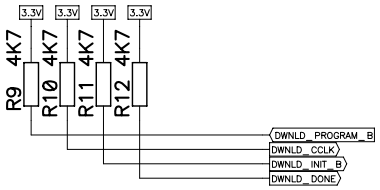
On mezzanine side



FPGA Done LED

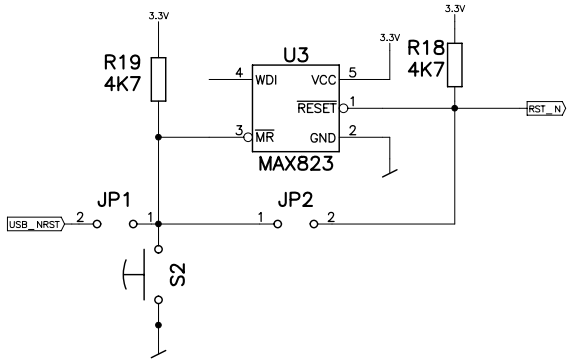
On mezzanine side





Reset circuit

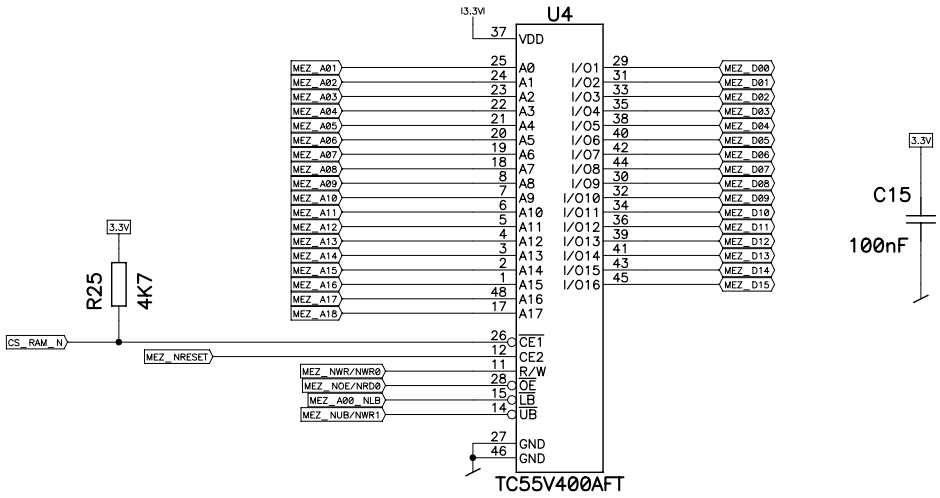
On motherboard side



FPGA_EBS Part : FPGA Config	DES	07.2002	Laurent Gauch
	REV	v1.1	12.06.2006 WAL
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS	3/10	...\FPGA-EBS\FPGA_EBS_V1.1 FPGA_EBS.sch	

RAM (256k*16)

On mezzanine side

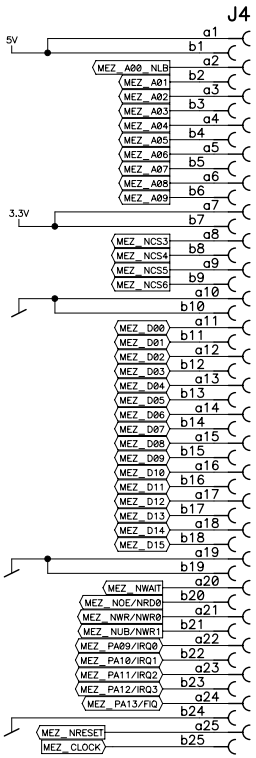


FPGA_EBS Part : Ram	DES	07.2002	Laurent Gauch
	REV	v1.1	12.06.2006 WAL
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS	4/10	...\FPGA-EBS\FPGA_EBS_V1.1 FPGA_EBS.sch	

Mezza A

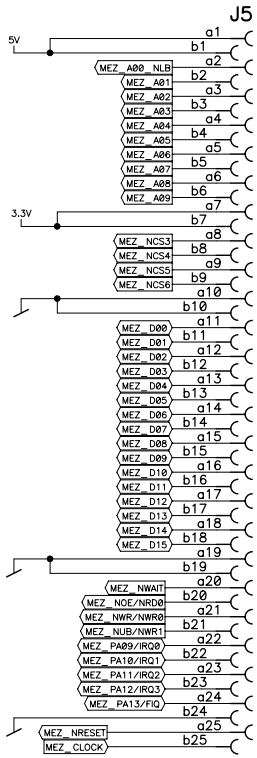
On mezzanine side

TOP SIDE



39 point-to-point IOs
+ 1 global reset
+ 1 global clock (CLOCK)

BOTTOM SIDE

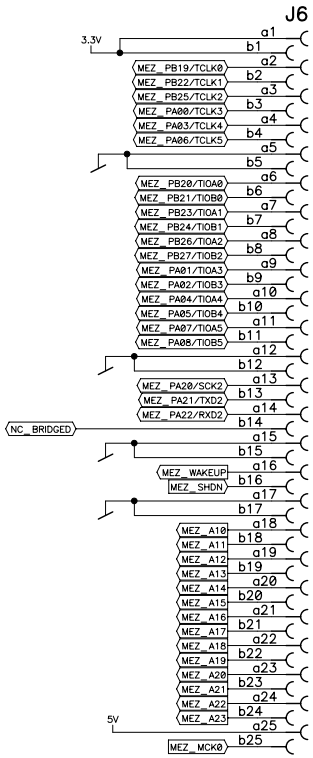


39 point-to-point IOs
+ 1 global reset
+ 1 global clock (CLOCK)

Mezza B

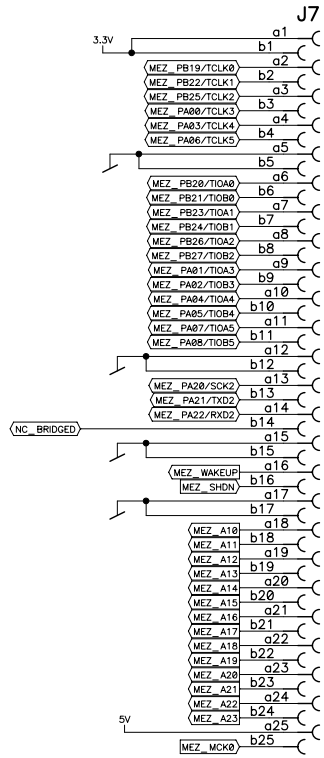
On mezzanine side

TOP SIDE



37 point-to-point IOs
+ 1 global clock (MCK0)

BOTTOM SIDE



37 point-to-point IOs
+ 1 global clock (MCK0)

FPGA_EBS Part : Mezzanine	DES	07.2002	Laurent Gauch
	REV	v1.1	12.06.2006 WAL
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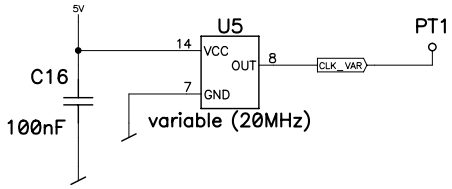
Crystal Oscillator

On motherboard side

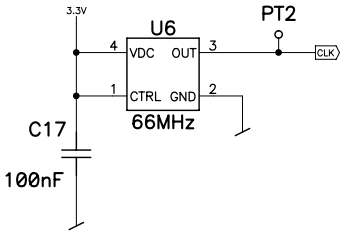
Frequency Output Test Point : FOTP VAR



Crystal Oscillator

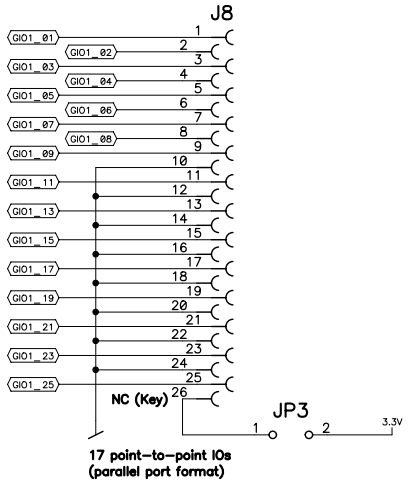
On mezzanine side

Frequency Output Test Point : FOTP 66MHz



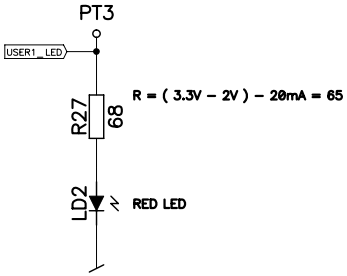
General purpose Connector

On mezzanine side



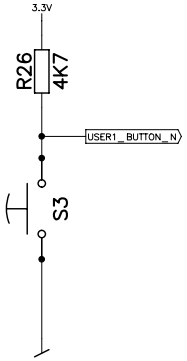
USER1 LED

On mezzanine side



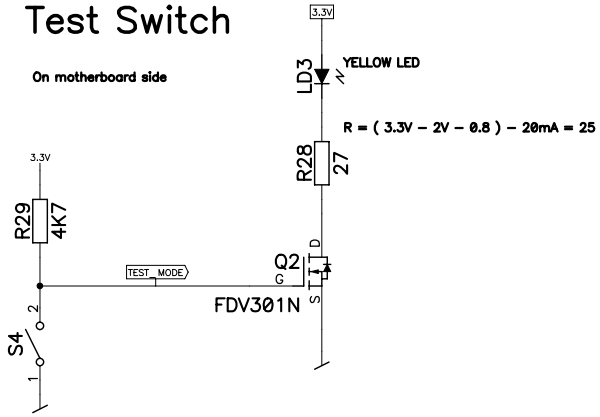
USER1 Button

On mezzanine side



Test Switch

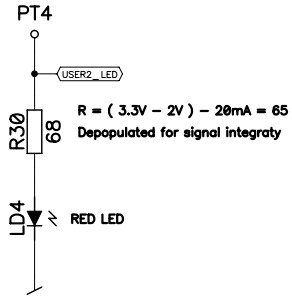
On motherboard side



USER2 LED

On mezzanine side

IO Test Point : TP IO



FPGA_EBS Part : Point-to-point IOs	DES	07.2002	Laurent Gauch
	REV	v1.1	12.06.2006 WAL
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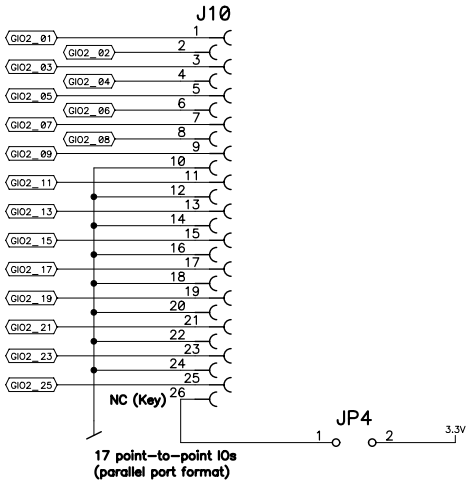
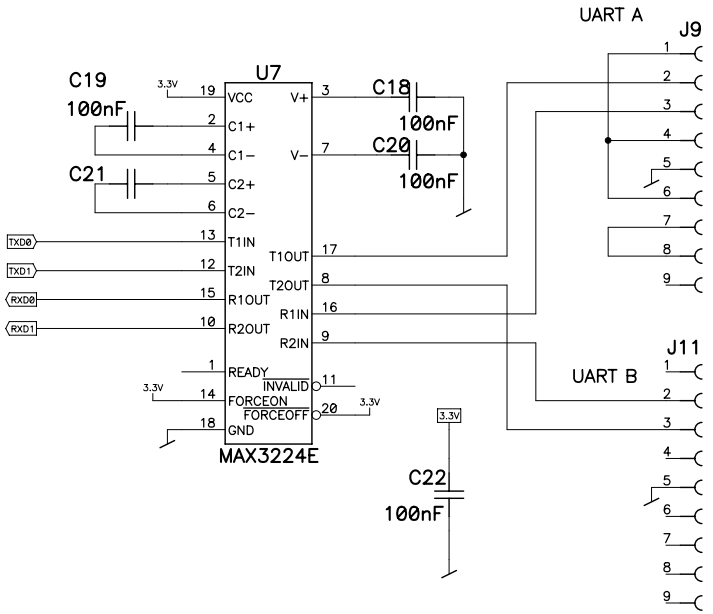
General purpose Connector

On mezzanine side



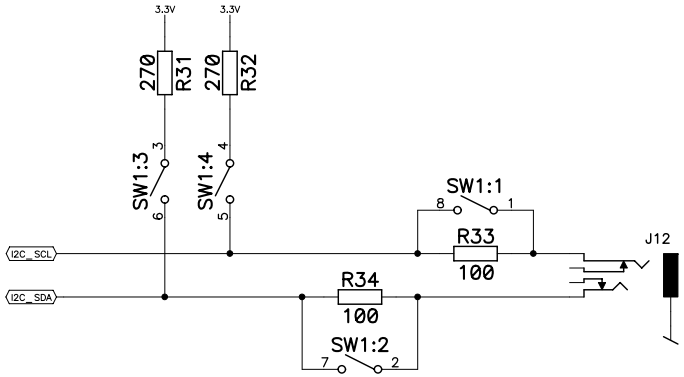
RS 232 Serial ports

On motherboard side



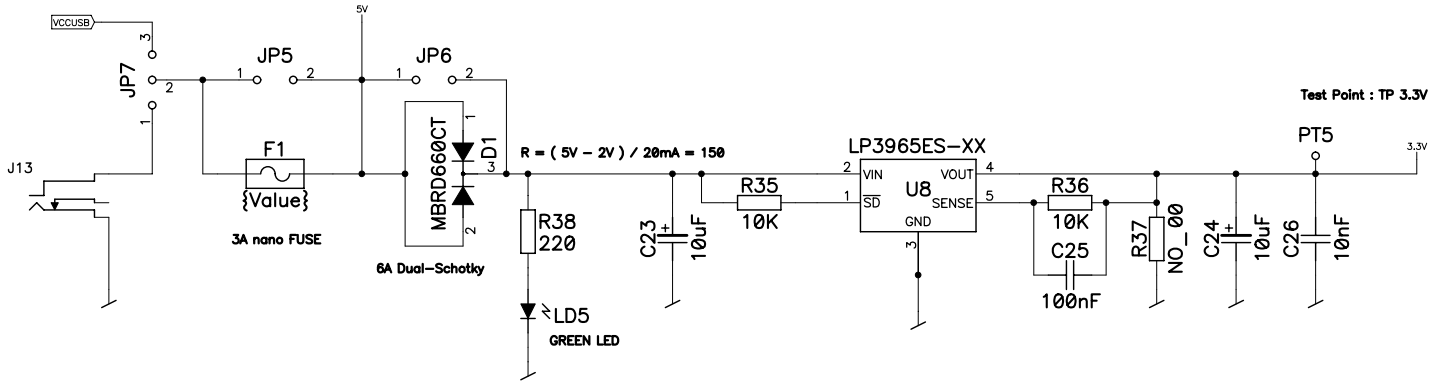
I2C or IRDA IO Connector

On motherboard side

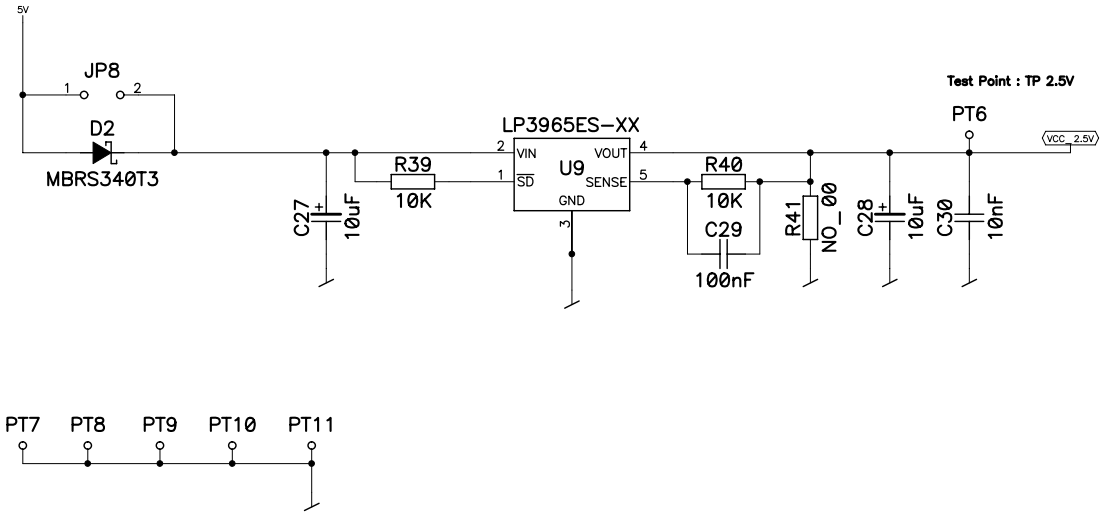


FPGA_EBS Part : Shared IOs	DES	07.2002	Laurent Gauch
	REV	v1.1	12.06.2006 WAL
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS	7/10	...\FPGA-EBS\FPGA_EBS_V1.1 FPGA_EBS.sch	

Power supply 3.3V/3A from 5V

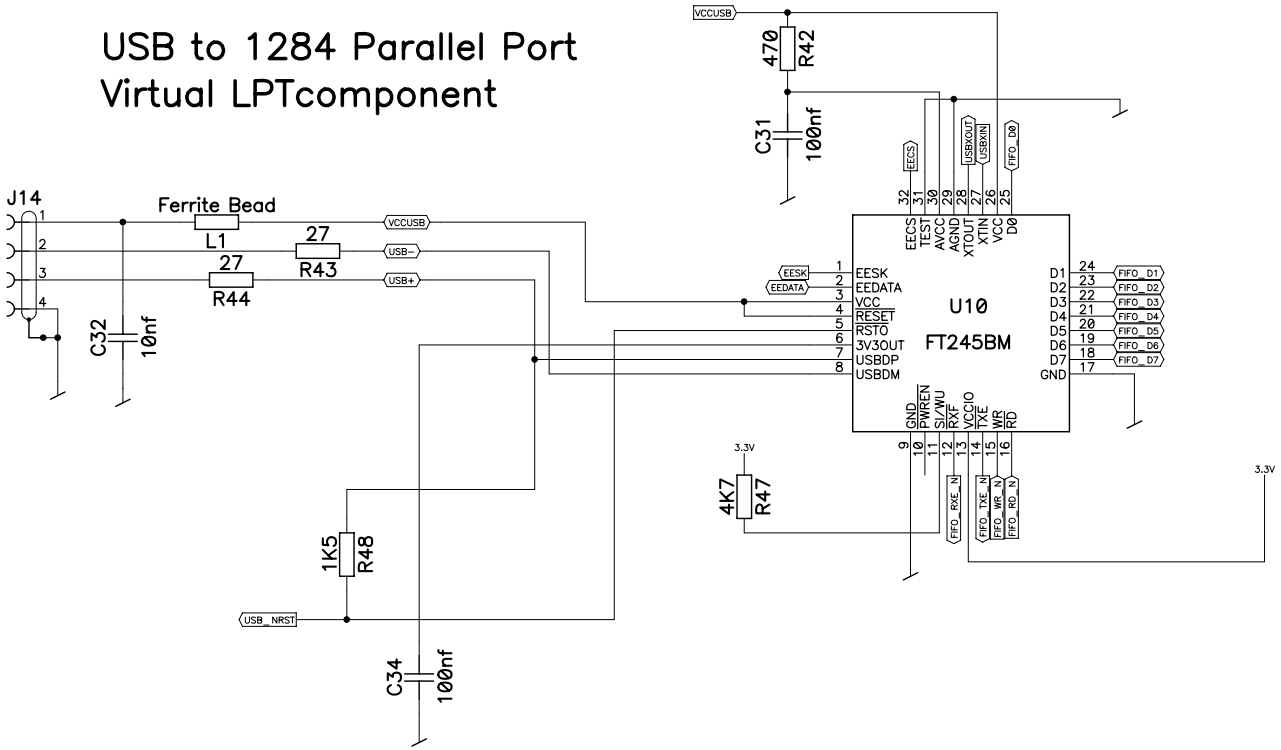


Power supply 2.5V/1.5A from 5V

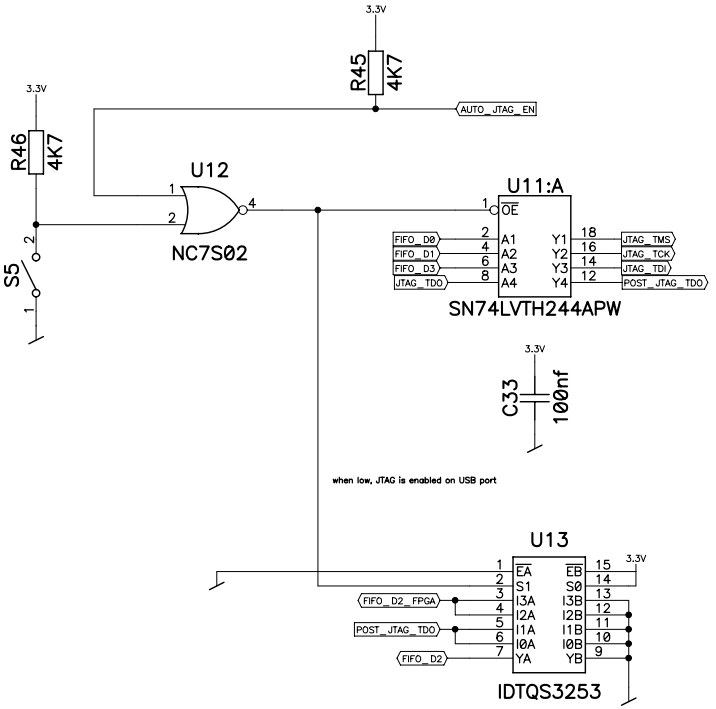


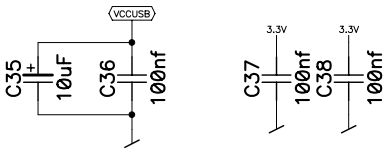
FPGA_EBS Part : Power	DES	07.2002	Laurent Gauch
	REV	v1.1	12.06.2006 WAL
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS	8/10	...\FPGA-EBS\FPGA_EBS_V1.1 FPGA_EBS.sch	

USB to 1284 Parallel Port
Virtual LPTcomponent

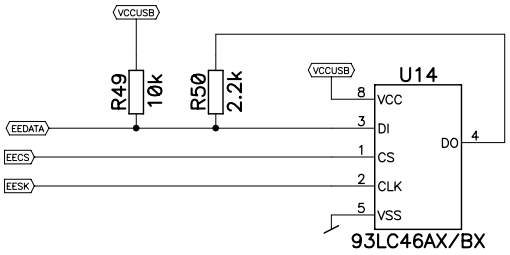


USB to JTAG

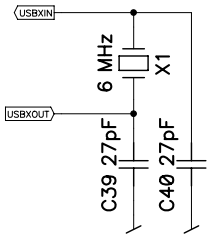




EEPROM
FOR USB
256 x 8



QUARTZ FOR USB



FPGA_EBS Part : USB	DES	07.2002	Laurent Gauch
	REV	v1.1	12.06.2006 WAL
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS	9/10	...\FPGA-EBS\FPGA_EBS_V1.1 FPGA_EBS.sch	