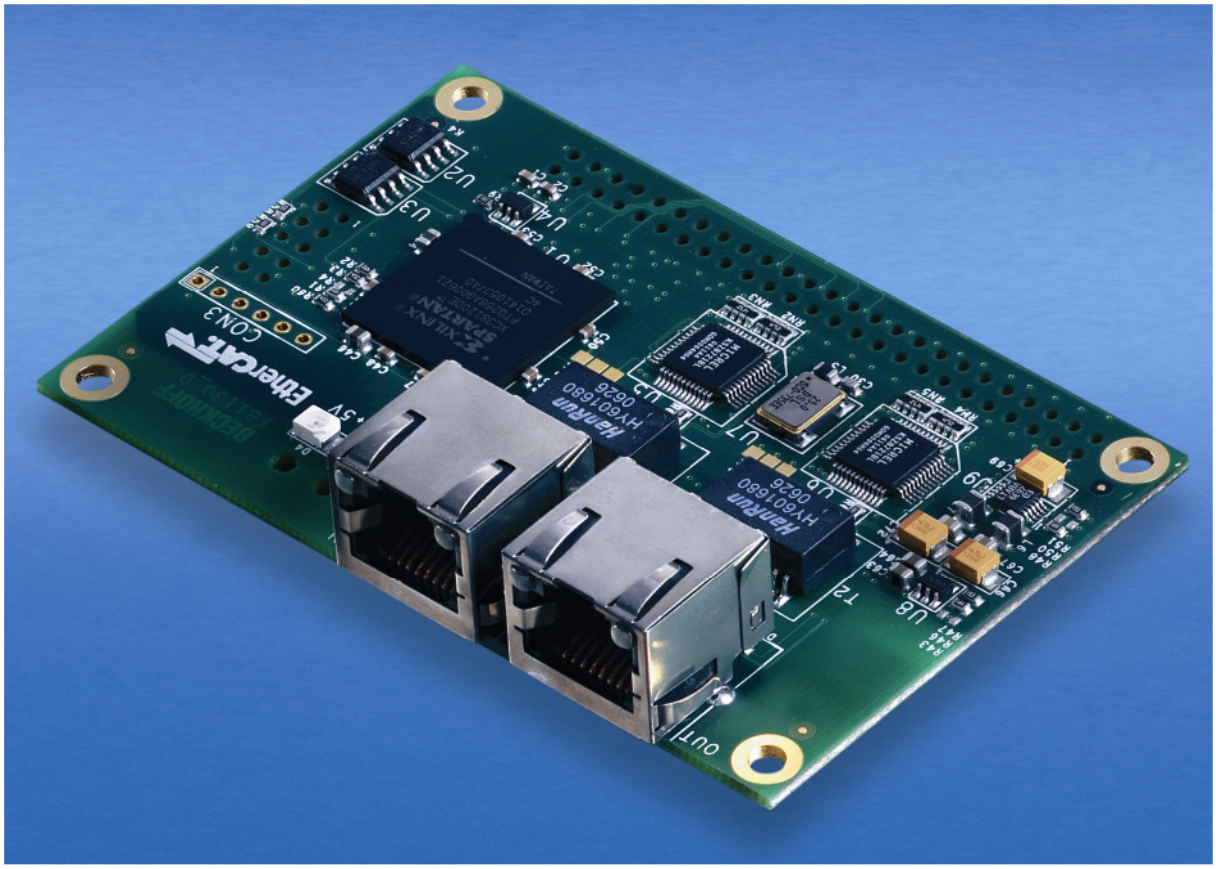

Hardware Data Sheet

FB1130

EtherCAT Piggyback Controller Boards

Version 1.5
Date: 2009-02-13

BECKHOFF

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TABLES

FIGURES

ABBREVIATIONS

DC	Direct Current
EEPROM	Electrically Erasable Programmable Read Only Memory. Non-volatile memory used to store ESC configuration and description.
ESC	EtherCAT Slave Controller
EtherCAT	Real-time Standard for Industrial Ethernet Control Automation Technology
GND-Earth	Ground-Earth
LED	Light Emitting Diode, used as an indicator
PCB	Printed Circuit Board
PDI	Process Data interface
SPI	Serial Peripheral Interface
RJ45	FCC Registered Jack, standard Ethernet connector (8P8C)

1 Foreword

1.1 Notes on the Documentation

This description is only intended for the use of trained specialists in control and automation engineering who are familiar with the applicable national standards. It is essential that the following notes and explanations are followed when installing and commissioning these components.

1.1.1 Liability Conditions

The responsible staff must ensure that the application or use of the products described satisfy all the requirements for safety, including all the relevant laws, regulations, guidelines and standards.

The documentation has been prepared with care. The products described are, however, constantly under development. For that reason the documentation is not in every case checked for consistency with performance data, standards or other characteristics. None of the statements of this manual represents a guarantee (Garantie) in the meaning of § 443 BGB of the German Civil Code or a statement about the contractually expected fitness for a particular purpose in the meaning of § 434 par. 1 sentence 1 BGB. In the event that it contains technical or editorial errors, we retain the right to make alterations at any time and without warning. No claims for the modification of products that have already been supplied may be made on the basis of the data, diagrams and descriptions in this documentation.

1.2 Safety Instructions

1.2.1 Safety Rules

The responsible staff must ensure that the application or use of the products described satisfy all the requirements for safety, including all the relevant laws, regulations, guidelines and standards.

1.2.2 State at Delivery

All the components are supplied in particular hardware and software configurations appropriate for the application. Modifications to hardware or software configurations other than those described in the documentation are not permitted, and nullify the liability of Beckhoff Automation GmbH.

1.2.3 Personnel Qualification

This description is only intended for the use of trained specialists in control and automation engineering who are familiar with the applicable national standards.

1.2.4 Description of Safety Symbols

The following safety symbols are used in this operating manual. They are intended to alert the reader to the associated safety instructions.

Danger This symbol is intended to highlight risks for the life or health of personnel.

Warning This symbol is intended to highlight risks for equipment, materials or the environment.

Note This symbol indicates information that contributes to better understanding.

1.3 Documentation Issue Status

Version	Comment
0.1	• First Version
1.0	• First official release
1.1	• Table for SPI programming interface added
1.2	• Figures 1, 5 and 6 updated
1.3	• Operating- and storage temperature recommendations
1.4	• 56 Pin CON1-Drawing and pin mapping tables changed.
1.5	• Changes in Table 7

2 Overview

The EtherCAT Piggyback controller board FB1130 combines a Xilinx FPGA, two EtherCAT ports and a PDI-Connector on a printed circuit board. Target applications for this Piggyback controller board are IP Core based EtherCAT devices with non standard process data interfaces (PDI). The board can as well be used for EtherCAT evaluation purposes as assembled in into customer end products.

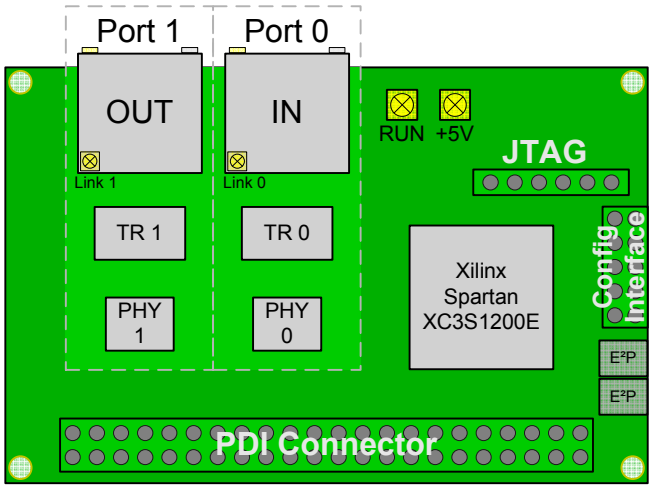

Figure 1: Overview of the FB1130

Key components on the FB1130 Piggyback controller are the EtherCAT ports 0 an 1, two EEPROMS, LEDs, a JTAG-Interface, a SPI Flash EEPROM in-circuit programming interface, the PDI connector and at last the Xilinx Spartan XC3S1200E FPGA.

2.1 EtherCAT Ports 0 an 1

The EtherCAT ports connect the FB1130 Piggyback controller board with the EtherCAT bus system. For the incoming EtherCAT data stream the port 0 is designated. Accordingly port 1 is assigned for the outgoing data stream. Standard CAT5-Cable can be used to interface with the Piggyback controller board. Especially suited EtherCAT cable can be found on the internet representation of the Beckhoff New Automation Company.

2.2 Indicator LEDs

According to the EtherCAT Indicator specification the FB1130 Piggyback controller board has four indicator LEDs in order to visualize Power- and Link-status as well as the state of the EtherCAT state machine.

Table 1: Indicator LEDs

LED	Comment
+5V	Indicates 5V power supply
RUN	RUN indicator (LED) for application state
Link 0	Link/Act Indicator (LED) for port 0
Link 1	Link/Act Indicator (LED) for port 1

States and flash rates of the RUN-LED can be found in the EtherCAT Indicator Specification that can be downloaded from the internet representation of the EtherCAT Technology Group.

2.3 Xilinx Spartan XC3S1200E

As well the EtherCAT IP Core as the application specific Process Data Interfaces are implemented on the Xilinx Spartan XC3S1200E FPGA. FPGA attributes as footprint and speed grade are shown in the following table.

Table 2 Parameters of the Xilinx Spartan XC3S1200E FPGA

FPGA Attributes	Value
System Gates	1,200K
Logic Cells	19,512
Dedicated Multipliers	28
Block RAM Blocks	28
Block RAM Bits	504K
Distributed RAM Bits	136K
DCMs	8
Package	FT(G)256
Speed Grade	-4
Temperature Rate	Commercial (0°C to 85°C)

Detailed, additional information of the Xilinx FPGA can be found on the Xilinx internet representation.

2.4 FPGA-Configuration EEPROM

For automatic start up of the IP Core the FB1130 Piggyback controller board brings up a FPGA Configuration EEPROM that can be programmed using the SPI in-circuit programming interface. The EEPROM type used on the FB1130 Piggyback controller board is the M25P40 from STMicroelectronics.

2.5 EtherCAT SII EEPROM

After the configuration of the FPGA the IP Core loads its configuration parameters out of the EtherCAT SII EEPROM. Detailed information about the content of the EEPROM can be found in the IP Core documentation. The EtherCAT SII EEPROM can be programmed over EtherCAT e.g. using TwinCAT.

2.6 JTAG-Interface

The JTAG header on the FB1130 Piggyback controller board is connected to the Xilinx FPGA for programming and debugging purposes. The JTAG header is only connected with the Xilinx FPGA, thus direct programming of the FPGA-Configuration EEPROM is not possible using this header. Later Versions of the Xilinx ISE Foundation will support programming the FPGA-Configuration EEPROM by using the JTAG indirect method.

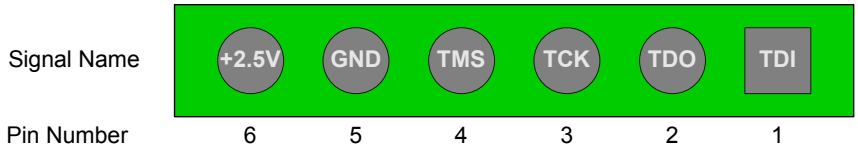

Figure 2: Pinout of the JTAG header

2.7 SPI Flash EEPROM in-circuit programming interface

Programming of the FPGA-Configuration EEPROM is supported by the SPI Flash EEPROM in-circuit programming interface (CON2) on the right side of the FB1130 PiggyBack controller board. When using the FB1130 together with the Evaluation Kit base board EL9800 this interface is automatically connected. In case of using the FB1130 Piggyback controller board in customer devices a SPI Flash EEPROM in-circuit programming interface has to be implemented and connected with the FB1130. Therefore the pinout of the SPI Flash EEPROM in-circuit programming interface from top side view is shown in Figure 3.

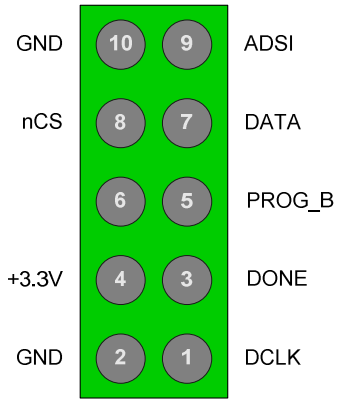

Figure 3 SPI Flash EEPROM in-circuit programming interface; Top side view.

In Table 3 the signal description of the connector CON2 is given.

Table 3: SPI interface signal description

Signal	Pin Type	Description
nCS	Input	Active low chip select
DATA	Output	Data output of SPI FLASH
ADSI	Input	Data input of SPI FLASH
DCLK	Input	Clock supply
DONE	Output	High, after configuration
PROG_B	Input	Forces reload of EEPROM
+3.3V	Power	Power pin connected to +3.3V
GND	Ground	Ground pin

2.7.1 SPI Flash EEPROM Feature Summary

- Device: M25P40
- 4 Mbit of Flash Memory
- SPI Bus Compatible Serial Interface
- 40MHz Clock Rate (maximum)
- 2.7 to 3.6V Single Supply Voltage

2.8 Test Pads

Three test pads associated to each PHY are available to monitor their TX-Enable and RX-DV signals. The pinout of these test pads are shown in the chapters 2.8.1f.

2.8.1 Port 0 – IN

Table 4: Port 0 Test Pads

Designator	Signal	Connected To
TP1	TX_ENABLE	U5 Pin 16
TP2	RX_DV	U5 Pin 9
TP3	GND	GND

2.8.2 Port 1 – OUT

Table 5: Port 1 Test Pads

Designator	Signal	Connected To
TP4	TX_ENABLE	U6 Pin 16
TP5	RX_DV	U6 Pin 9
TP6	GND	GND

3 PDI-Connector

The Process Data Interface of the IP Core can be accessed via a dual row (2 x 25 pin) PDI-Connector (CON1). Additionally power supply signals are placed on this connector. The distribution of the power pins is shown in chapter 3.1. In Chapter 3.2 an overview over the mapping between PDI connector pin and IP Core port is given.

3.1 Power Supply

Figure 3.1 shows the distribution of the power pins on the PDI Connector from top side view.

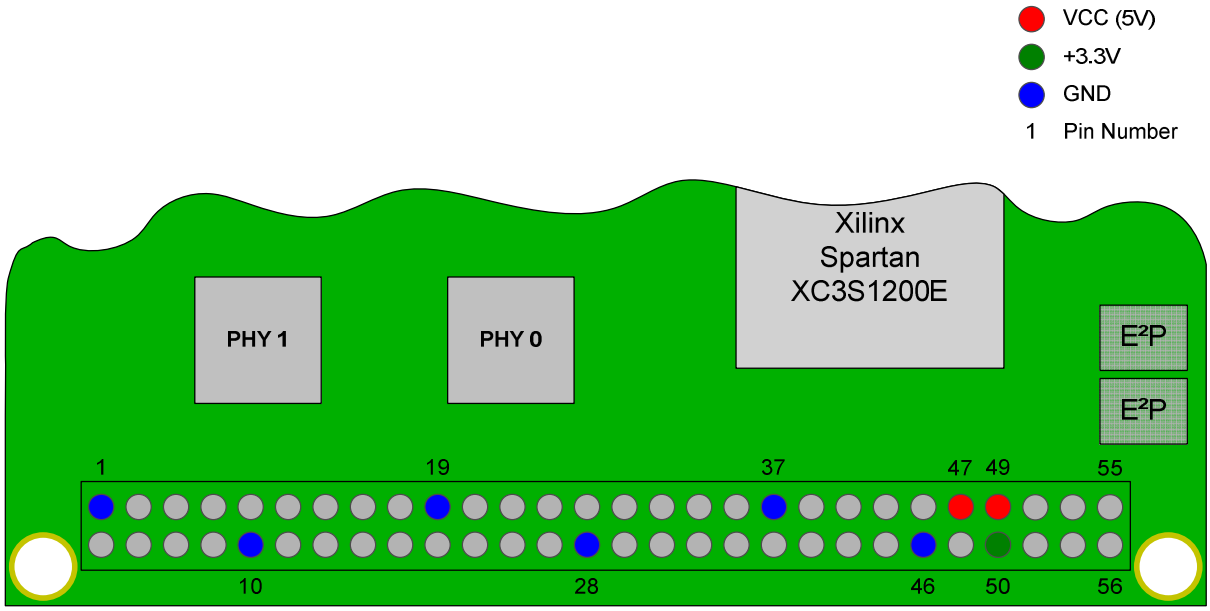

Figure 4: PDI Connector Power Pin Distribution

Pins 47 and 49 have to be supplied with +5V $V_{CC.}$ Pin 50 is a 3.3V Output from one DC-DC converter on the FB1130. The maximum current that can be driven through the 3.3V output (Pin 50) is limited to 100mA. The GND pins, which are marked blue, have to be connected to a ground plane on the supplying PCB.

3.2 Port to Pin Mapping between IP Core and PDI-Connector

Table 6 FPGA Pin to PDI connector mapping

Pin number	Port	FPGA Pin
1	GND	
2	PA0	G16
3	PA1	G15
4	PA2	H15
5	PA3	J16
6	PA4	K16
7	PA5	K15
8	PA6	L15
9	PA7	M16
10	GND	
11	PB0	N15
12	PB1	N16
13	PB2	P16
14	PB3	P15
15	PB4	R16
16	PB5	R15
17	PB6	P13
18	PB7	N12
19	GND	
20	PC0	P12
21	PC1	P11
22	PC2	R11
23	PC3	P10
24	PC4	R10
25	PC5	P8
26	PC6	T8
27	PC7	N7
28	GND	

Pin number	Port	FPGA Pin
29	PD0	P7
30	PD1	N6
31	PD2	P6
32	PD3	R6
33	PD4	T5
34	PD5	R4
35	PD6	T4
36	PD7	R2
37	GND	
38	PE0	R1
39	PE1	P2
40	PE2	P1
41	PE3	N1
42	PE4	M1
43	PE5	M4
44	PE6	L3
45	PE7	L2
46	GND	
47	VCC	
48	N.C.	
49	VCC	
50	3.3V Out	
51	PF0	G14
52	PF1	F12
53	PF2	H14
54	PF3	L14
55	PF4	K14
56	PF5	J14

4 Xilinx IP Core

As mentioned above, target application for the FB1130 Piggyback controller board is the operation in combination with the EtherCAT IP Core for Xilinx FPGAs. All necessary information about configuration, synthesis and mapping of the IP Core are listed in the *ET1815/ET1817 EtherCAT IP core for Xilinx FPGAs* documentation that can be downloaded from the company's website.

4.1 16bit digital Input / 16bit digital Output demonstration mode

For demonstration purposes only, the FB1130 Piggyback controller board comes up together with a synthesized IP Core bitstream, which provides a 16bit digital Input/16bit digital Output PDI interface. This IP Core bitstream, initially stored in the FPGA-Configuration EEPROM, is for test purposes only. It is not allowed to be used in end customer products.

4.1.1 Signal mapping for 16bit digital Input/Output and PDI-Connector

Table 7: Signal mapping 16bit digital Input/Output

Pin number	Port	Signal
1	GND	
2	PA0	INPUT[0]
3	PA1	INPUT[1]
4	PA2	INPUT[2]
5	PA3	INPUT[3]
6	PA4	INPUT[4]
7	PA5	INPUT[5]
8	PA6	INPUT[6]
9	PA7	INPUT[7]
10	GND	
11	PB0	INPUT[8]
12	PB1	INPUT[9]
13	PB2	INPUT[10]
14	PB3	INPUT[11]
15	PB4	INPUT[12]
16	PB5	INPUT[13]
17	PB6	INPUT[14]
18	PB7	INPUT[15]
19	GND	
20	PC0	OUTPUT[0]
21	PC1	OUTPUT[1]
22	PC2	OUTPUT[2]
23	PC3	OUTPUT[6]
24	PC4	OUTPUT[4]
25	PC5	OUTPUT[5]
26	PC6	OUTPUT[6]
27	PC7	OUTPUT[7]
28	GND	

Pin number	Port	Signal
29	PD0	OUTPUT[8]
30	PD1	OUTPUT[9]
31	PD2	OUTPUT[10]
32	PD3	OUTPUT[11]
33	PD4	OUTPUT[12]
34	PD5	OUTPUT[13]
35	PD6	OUTPUT[14]
36	PD7	OUTPUT[15]
37	GND	
38	PE0	Not Used
39	PE1	Not Used
40	PE2	Not Used
41	PE3	Not Used
42	PE4	Not Used
43	PE5	Not Used
44	PE6	Not Used
45	PE7	Not Used
46	GND	
47	VCC	
48	N.C.	
49	VCC	
50	3.3V Out	
51	PF0	Not Used
52	PF1	Not Used
53	PF2	Not Used
54	PF3	Not Used
55	PF4	Not Used
56	PF5	Not Used

5 Electrical Specification

5.1 Ratings

Table 8: Typical Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Board Supply Voltage		4.5	5.0	5.5	V
I_{CC}	Board Supply Current	1 Port 2 Ports	210	220 250	700	mA
$\vartheta_{Storage}$	Storage temperature		-65		105	°C
$\vartheta_{Ambient}$	Ambient temperature		-40		70	°C

5.2 EMC – Electro magnetic compatibility

For proper protection against damage caused by electrostatic discharge, the top left mounting hole of the EtherCAT piggyback controller board has to be connected to a massive panel or plate that is connected with GND-Earth. The remaining three holes have to be used for mechanical fixation of the piggyback controller board.

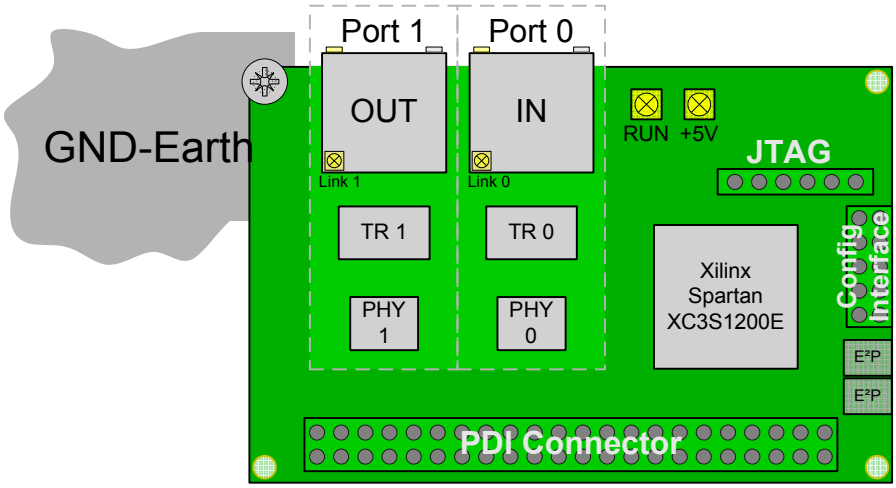

Figure 5: Connection to GND-Earth

Suitable screw dimensions are: M3x6 DIN-7985.

6 Mechanical Specification

As the EtherCAT piggyback controller board FB1130 can be assembled with customer hardware to complex end user devices, board dimensions and assembly recommendations have to be taken in account. In section 6.1 the board dimensions including mounting and contact hole positions and diameters from top view are shown. Panel opening recommendations are shown in section 6.3. All dimensions are drawn in millimeters.

6.1 Board Dimensions

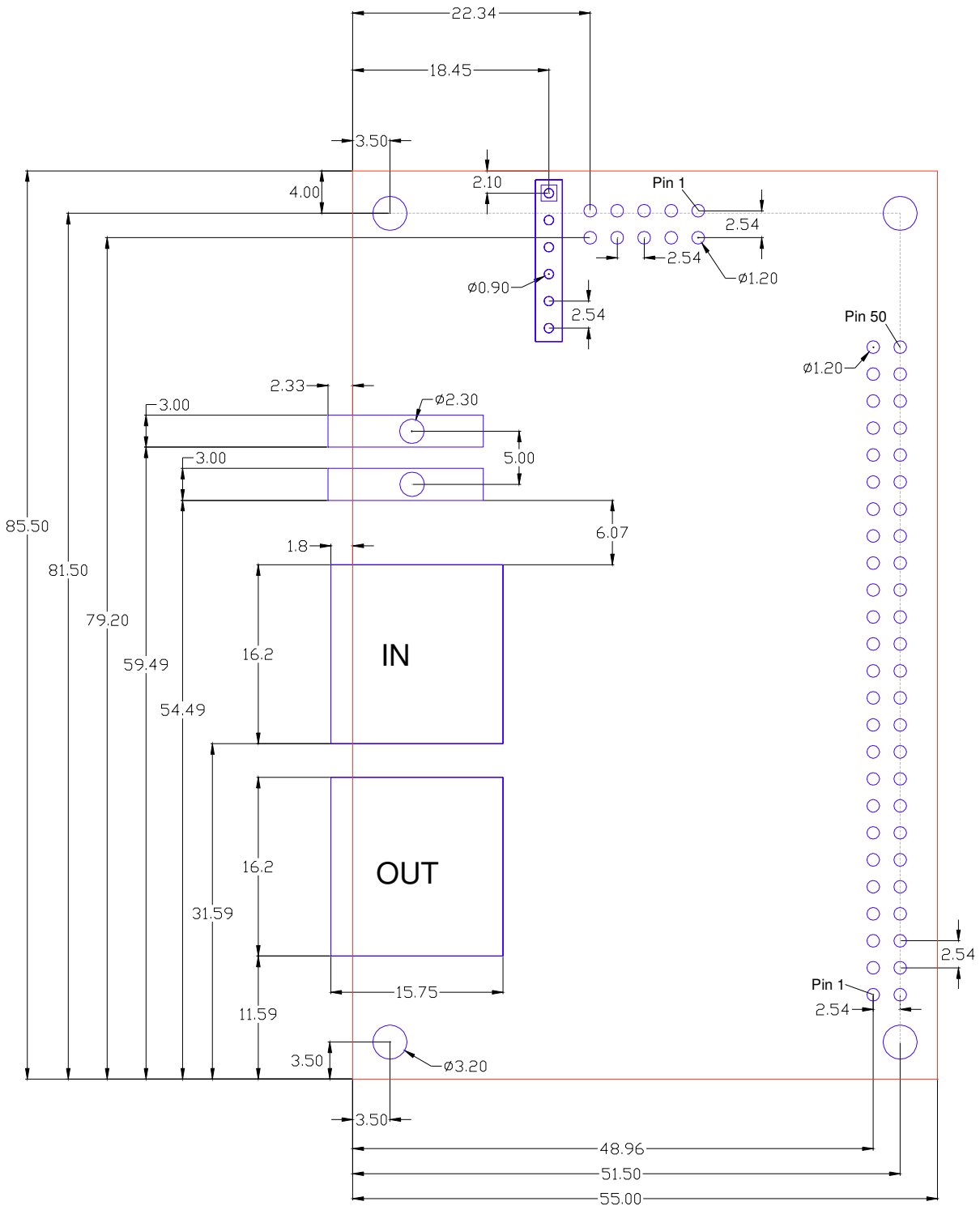

Figure 6: Board dimensions of the FB1130 – Top View

6.2 Physical Connector Specification

The Board to Board connector (*CON1*) can be connected as well from the bottom as from the top side of the FB1130. The bottom side low profile socket is equivalent to the *Samtec* (www.samtec.com) product with the manufacturer number CLH-125-F-D-BE-P-TR. Insertion depth from top side is 4.7 mm, respectively 3.2 mm from bottom side. A suitable pin header for the low profile socket can also received from *Samtec*. The TSM series is suitable for the socket. As an example the pin header with the part number TSM-125-02-L-DV can be used to connect the EtherCAT piggyback controller board FB1130.

6.3 Recommended Panel Opening

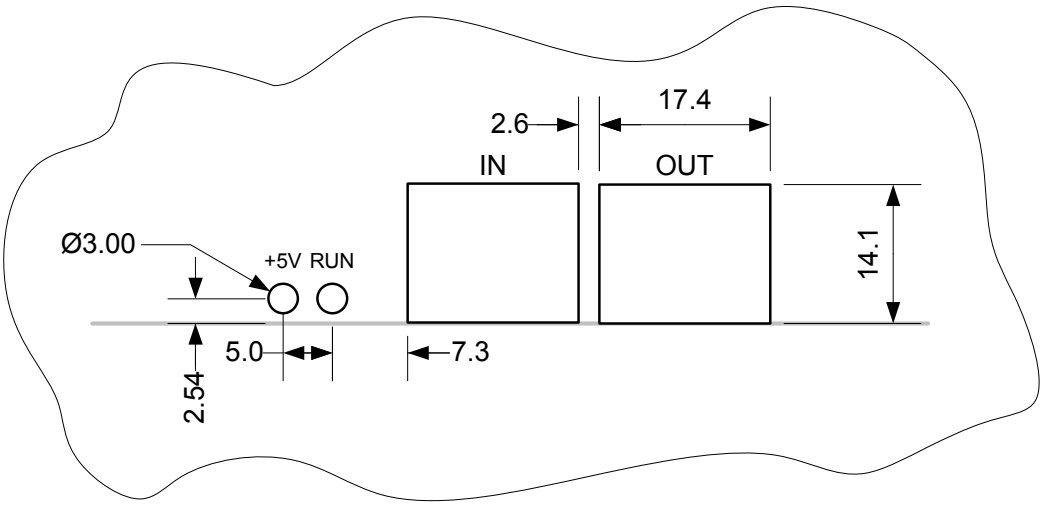

Figure 7: Recommended Panel Opening

In Figure 7 the dimensions of a typical panel opening is illustrated. The two ports and the LED break throughs have to be labelled as shown in the figure.

6.4 Top/Bottom Side Component Height Definition

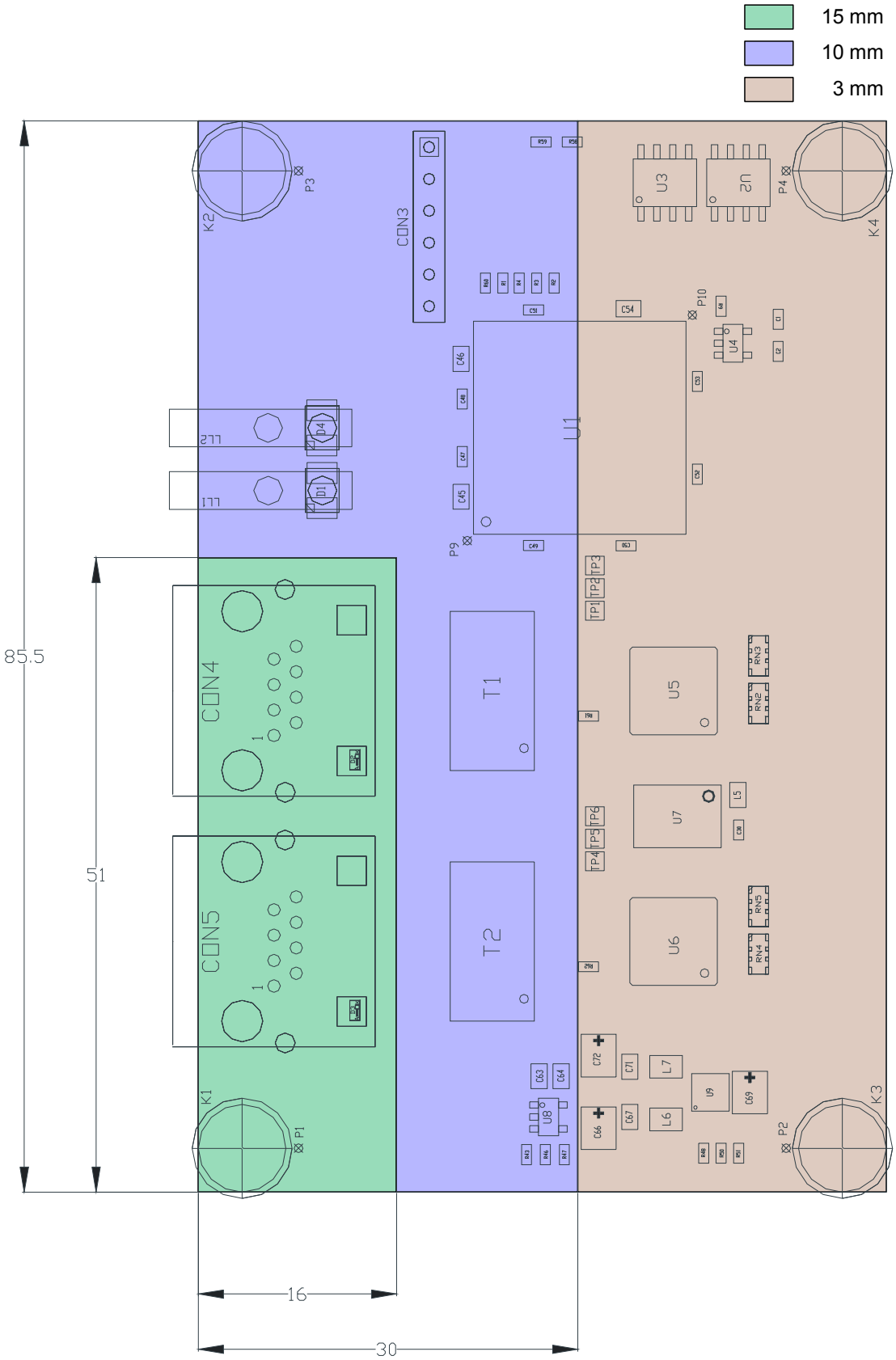

Figure 8: Component height zones for the top side of FB1130

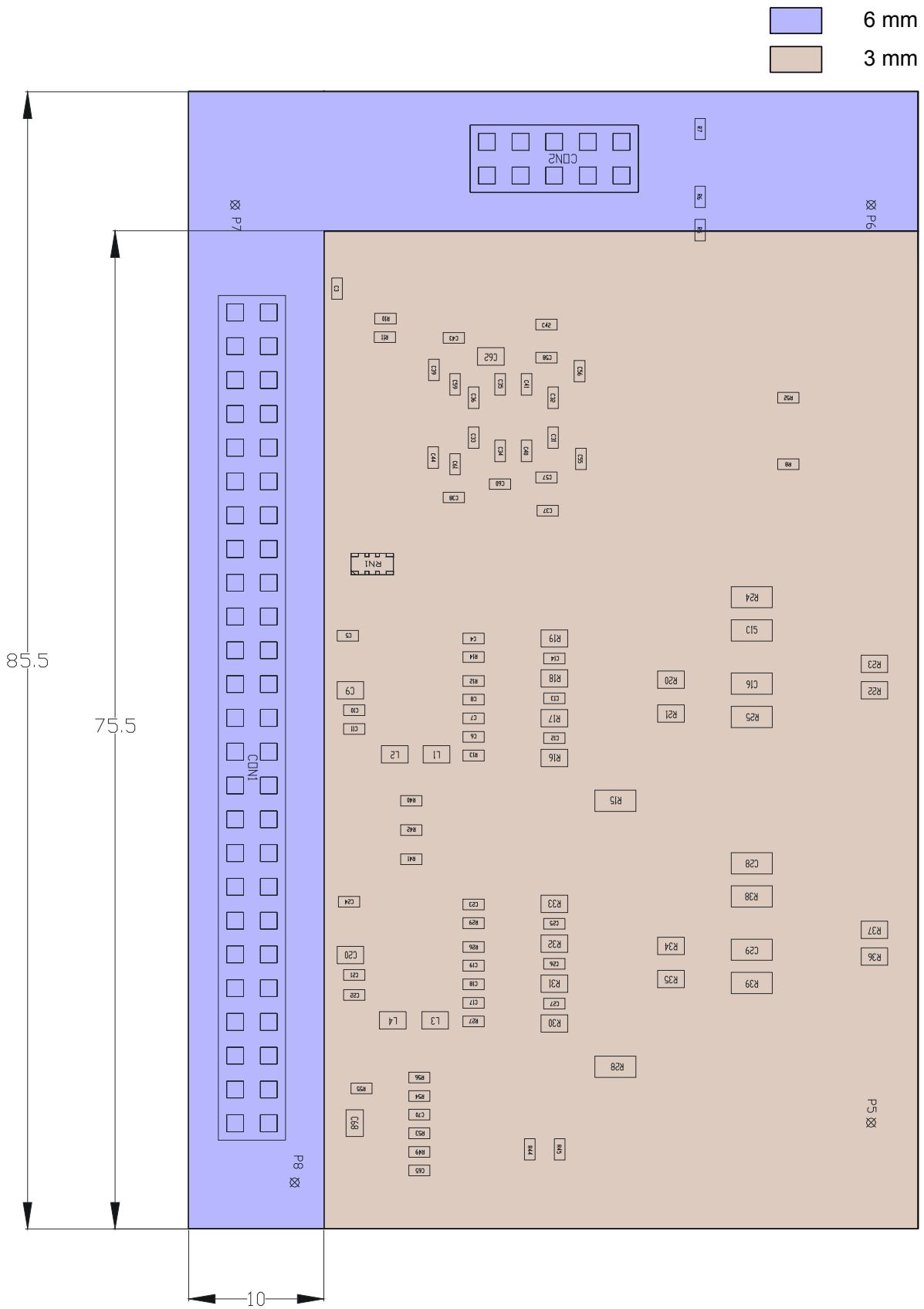

Figure 9: Component height zones for the bottom side of FB1130

7 Appendix

7.1 Support and Service

Beckhoff and their partners around the world offer comprehensive support and service, making available fast and competent assistance with all questions related to Beckhoff products and system solutions.

7.1.1 Beckhoff's branch offices and representatives

Please contact your Beckhoff branch office or representative for local support and service on Beckhoff products!

The addresses of Beckhoff's branch offices and representatives round the world can be found on her internet pages: http://www.beckhoff.com

You will also find further documentation for Beckhoff components there.

7.2 Beckhoff Headquarters

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