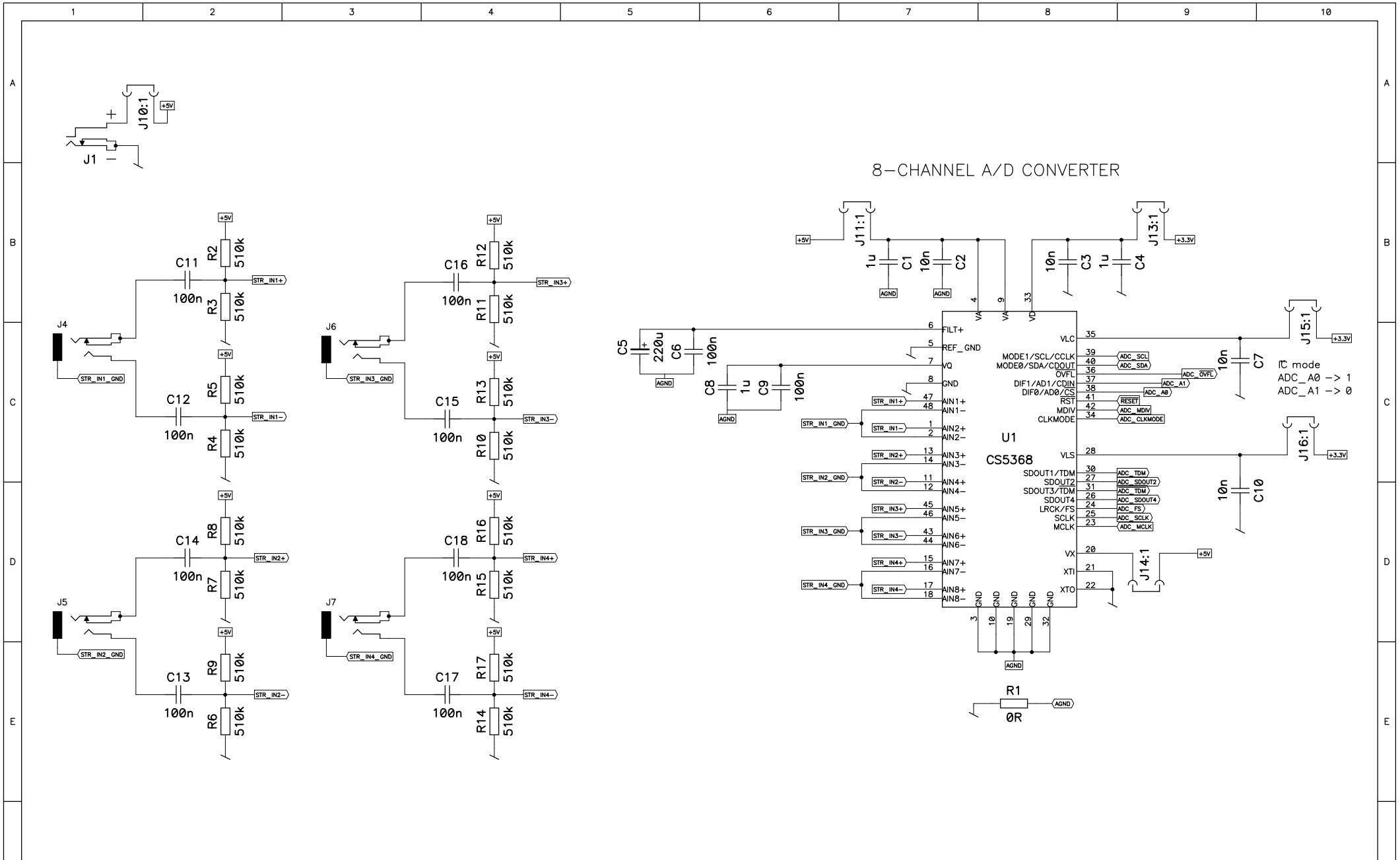
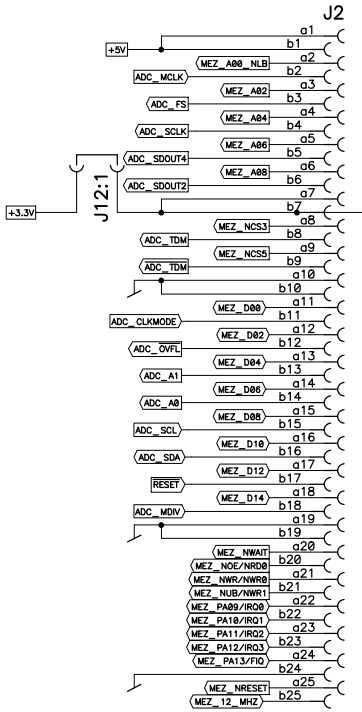


ADC_FPGA Adapter	Alimentation	DES	13.02.2012 SZUL
		REV	v1.0
HAUTE ECOLE VALAISANNE		1/2	I:Filiere\Promotion\EMVs\PCB Mezza_v1.0.sch

Mezza A

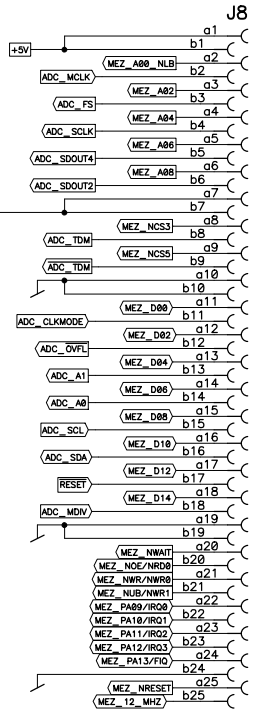
On mezzanine side

TOP SIDE



39 point-to-point IOs
+ 1 global reset
+ 1 global clock (CLOCK)

BOTTOM SIDE

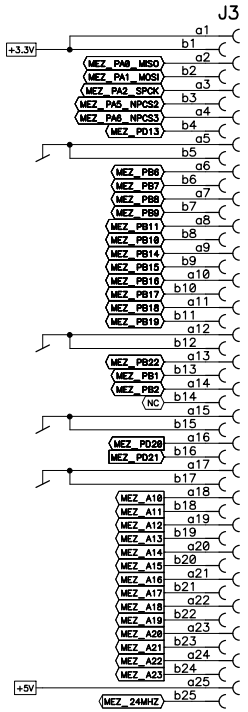


39 point-to-point IOs
+ 1 global reset
+ 1 global clock (CLOCK)

Mezza B

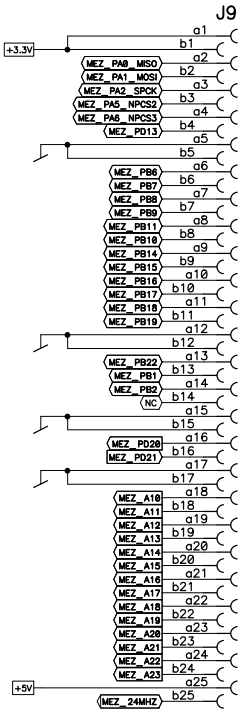
On mezzanine side

TOP SIDE



37 point-to-point IOs
+ 1 global clock (MCK0)

BOTTOM SIDE



37 point-to-point IOs
+ 1 global clock (MCK0)

ADC_FPGA Adapter Connecteur	DES	13.02.2012 SZUL
	REV	v1.0
HAUTE ECOLE VALAISANNE	2/2	I:Filiere\Promotion\EMVs\PCB Mezza_v1.0.sch