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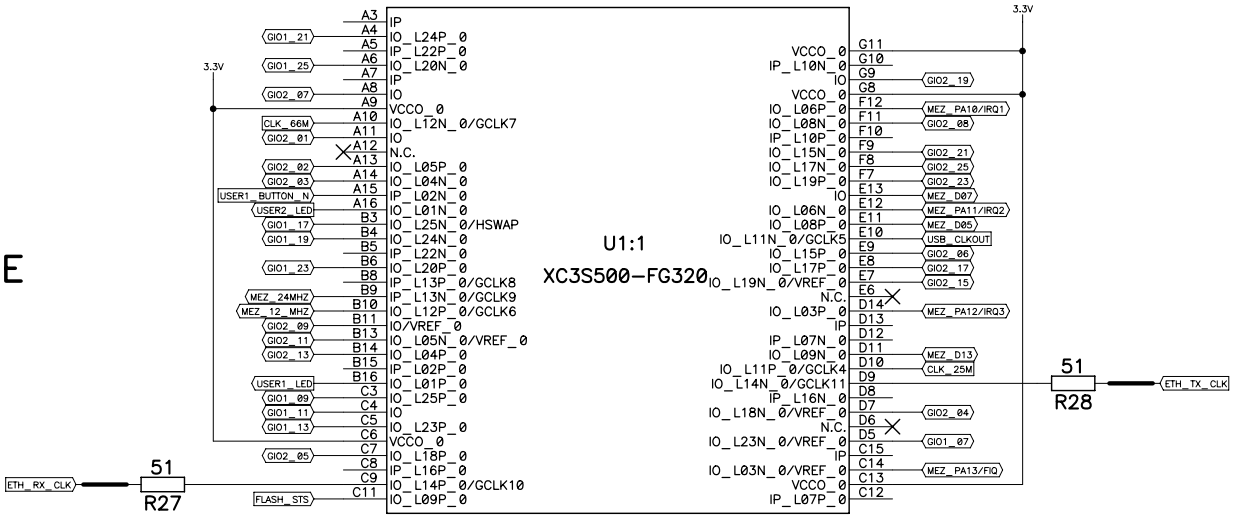
FPGA_ EBS Board : Educative FPGA platform

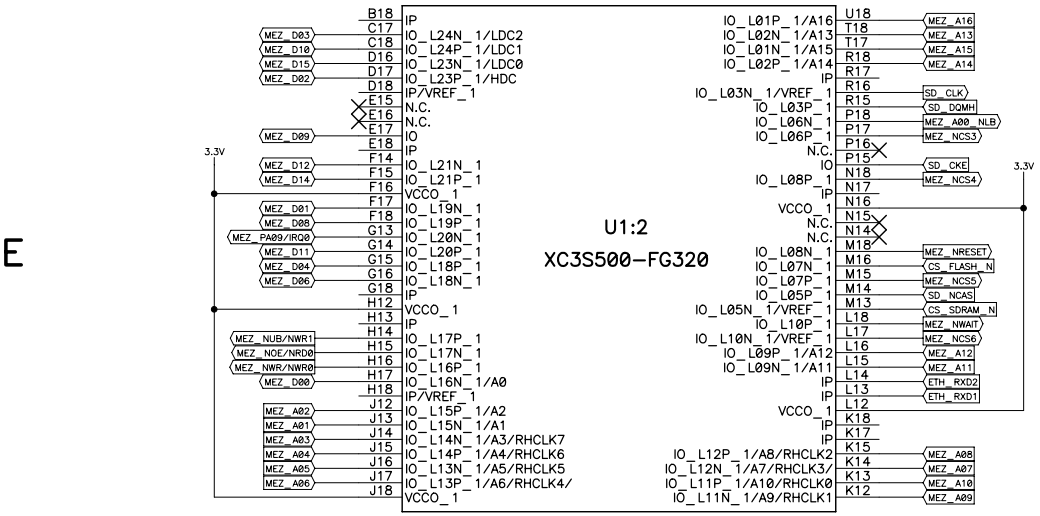
Page	Title	Description
1	Cover	This first page
2	FPGA 1	Xilinx SPARTAN–III FPGA Bank 0 & 1 / Configuration Mode
3	FPGA 2	Xilinx SPARTAN–III FPGA Bank 2 & 3 / Configuration Mode
4	FPGA Alim	Xilinx SPARTAN–III FPGA Alimentation / Decoupling Capacitances
5	FPGA Config	Xilinx EEPROM / JTAG Connectors / FPGA Done LED / Reset Circuit / Source of FPGA programmation
6	Memory	FLASH / SDRAM / Decoupling Capacitances
7	Mezzanine	Mezza A and Mezza B Connectors (mezzanine support)
8	Point–to–point IOs	Crystal Oscillators / User LED / User Button / Test Point / General Purpose connectors
9	Ethernet / RS232	RS232 Circuit / Ethernet interface and Power Over Ethernet
10	Power 1	Power Jack Connector / Voltage Detection / DC DC 5V
11	Power 2	3.3V, 2.5V and 1.2V regulation
12	USB	USB / FPGA dialog over USB / FPGA JTAG over USB

FPGA
SPARTAN – III series
FG320

BANK0
TOP SIDE

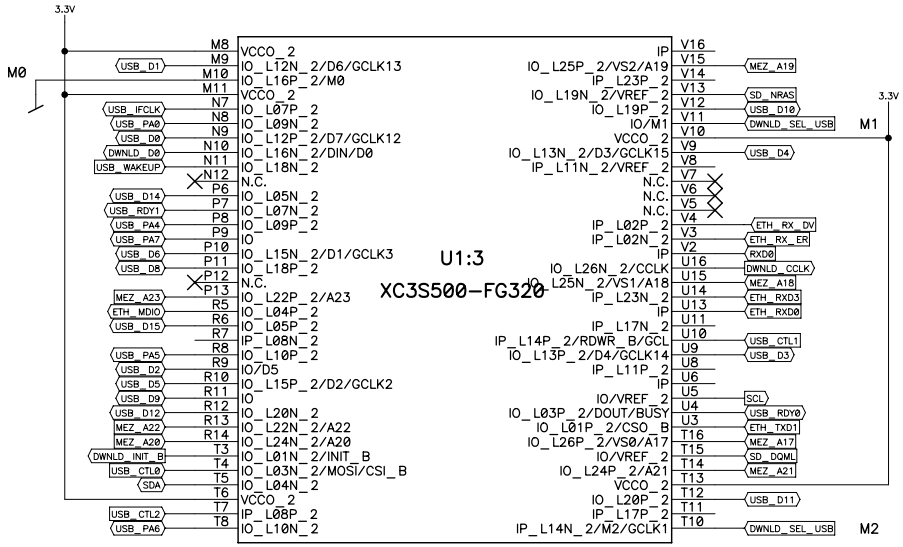


BANK1
RIGHT SIDE



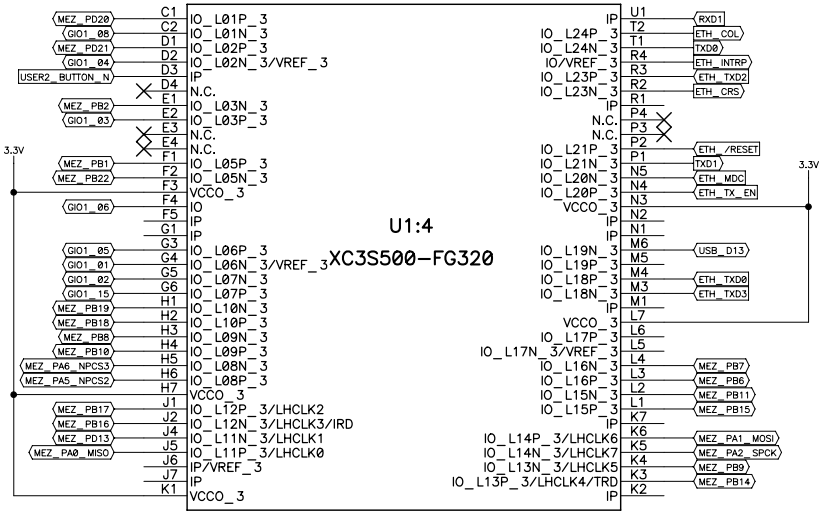
FPGA_EBS Part : FPGA 1		DES	02.2008 Valentini Samuel
		REV	{Revision}
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS		2/13	...\FPGA-EBS\FPGA_EBS_V1.1 FPGA_EBS_V2_0.sch

BANK2
BOTTOM SIDE



M2 M1 M0
0 0 0 : Master Serial (EEPROM)
1 1 0 : Slave paralell (USB2)

BANK3
LEFT SIDE



FPGA_EBS Part : FPGA 2		DES	02.2008 Valentini Samuel
		REV	{Revision}
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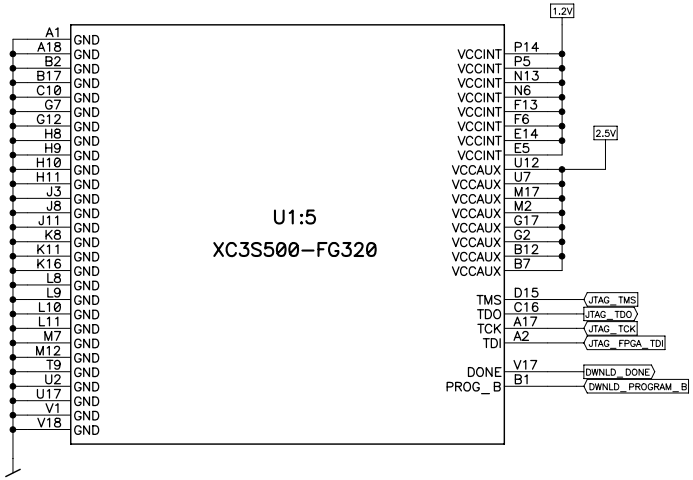
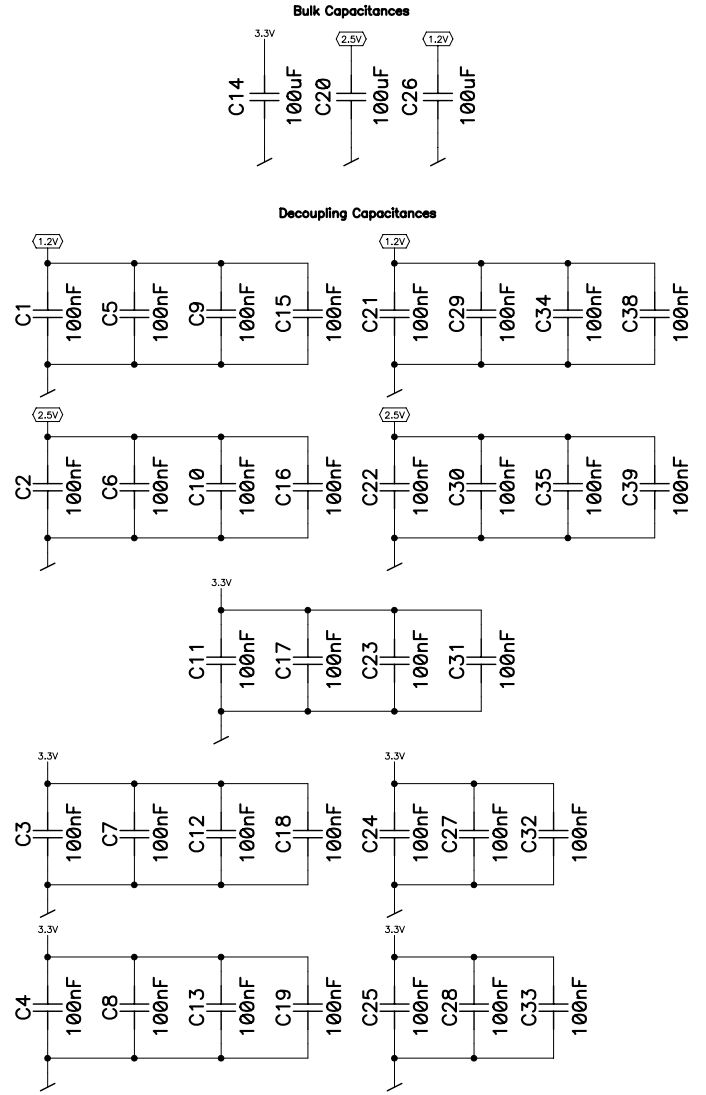
FPGA Capacitances

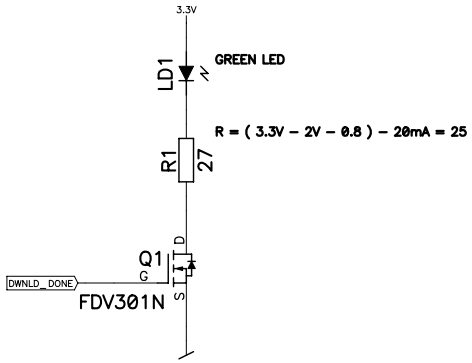




FPGA_EBS Part : FPGA Alim		DES	02.2008 Valentini Samuel
		REV	{Revision}
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS		4/13	...\FPGA-EBS\FPGA_EBS_V1.1 FPGA_EBS_V2_0.sch

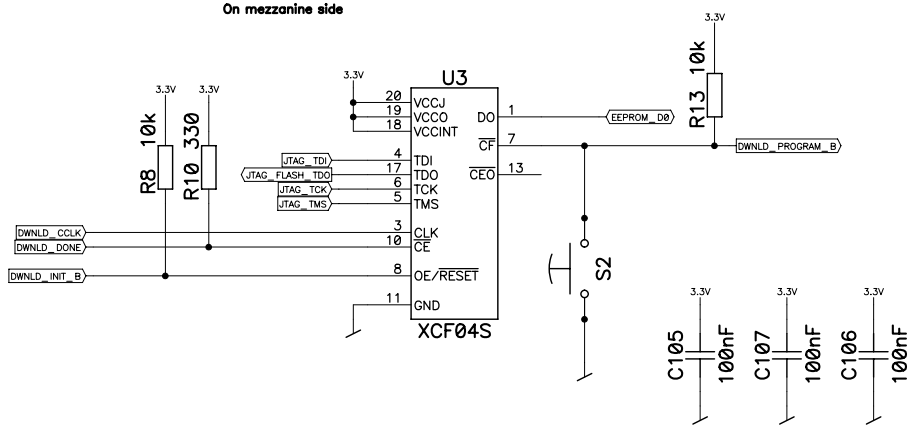
FPGA Done LED

On mezzanine side



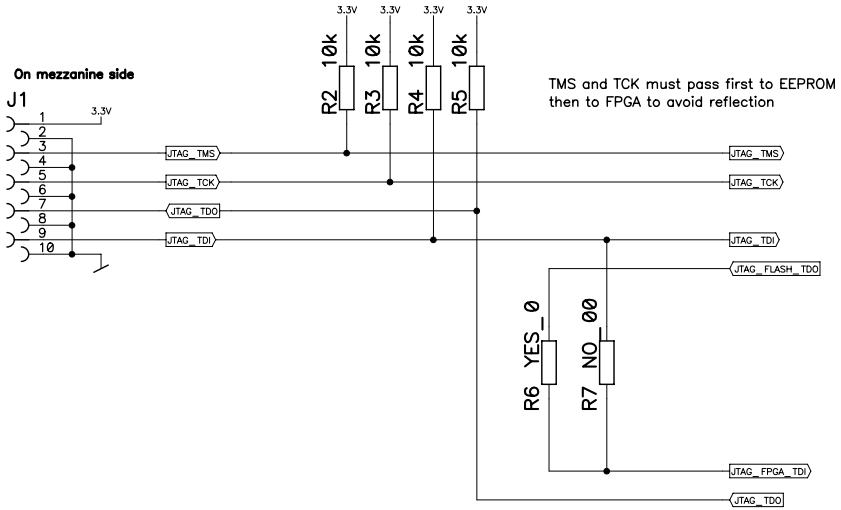
EEPROM for FPGA Configuration

On mezzanine side



JTAG connector

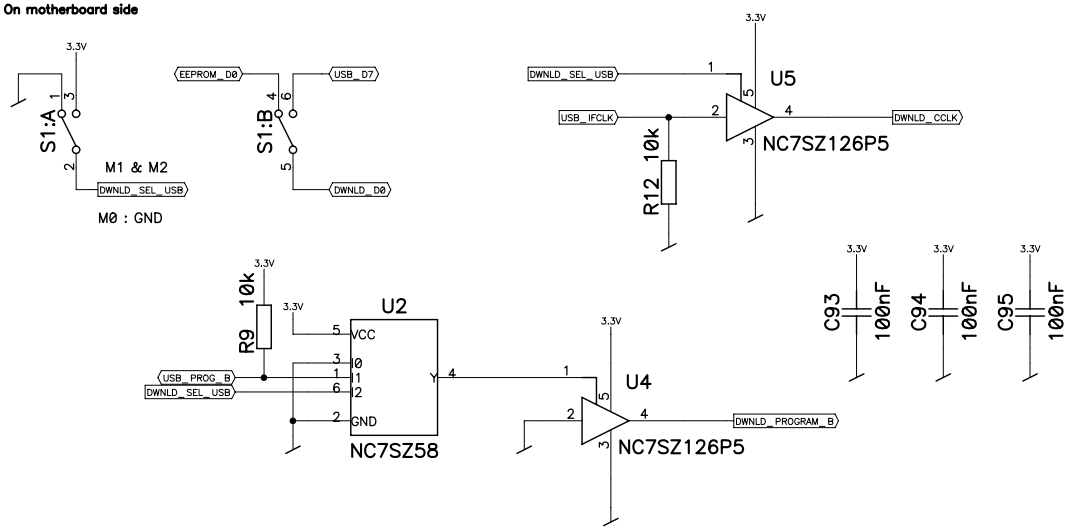
On mezzanine side



Source of programmation of the FPGA

0 0 0 : Master Serial (EEPROM)
1 1 0 : Slave paralell (USB2)
M2 M1 M0

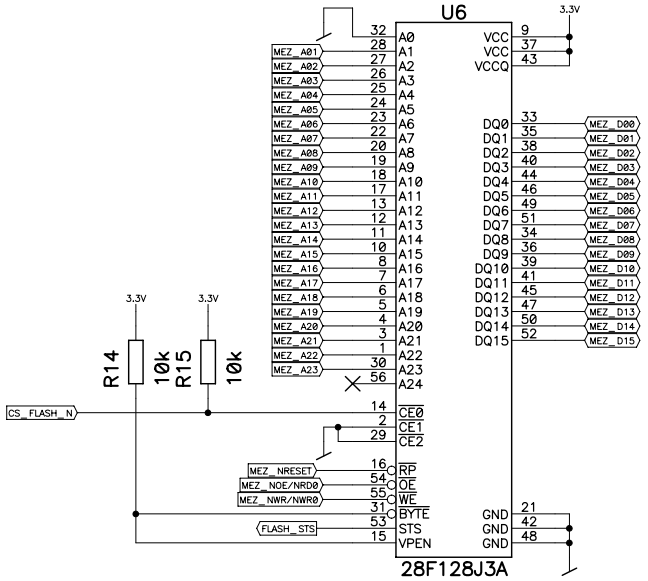
On motherboard side

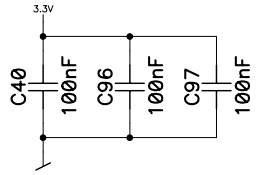


FPGA_EBS Part : FPGA Config		DES	02.2008 Valentini Samuel
		REV	{Revision}
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS		5/13	...\FPGA-EBS\FPGA_EBS_V1.1 FPGA_EBS_V2_0.sch

FLASH

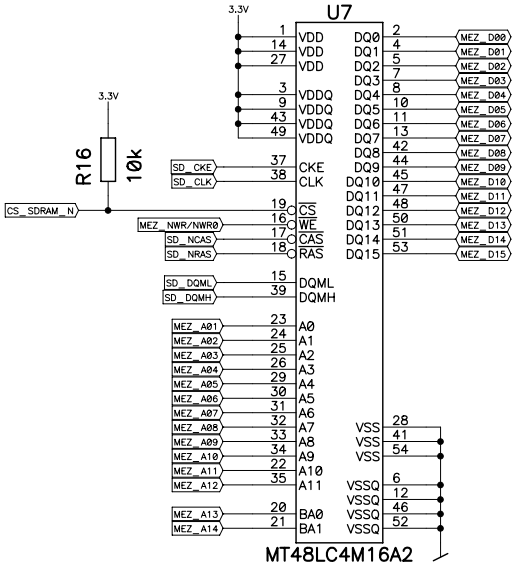
On mezzanine side

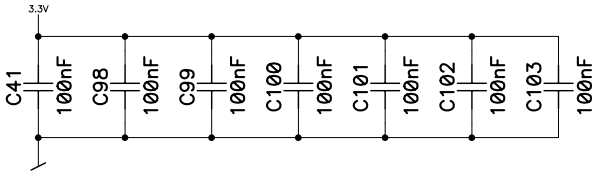




SDRAM

On mezzanine side



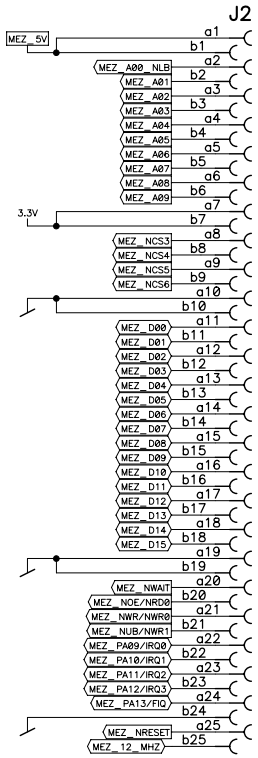


FPGA_EBS Part : Memory		DES	02.2008 Valentini Samuel
		REV	{Revision}
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS		6/13	...\FPGA-EBS\FPGA_EBS_V1.1\FPGA_EBS_V2_0.sch

Mezza A

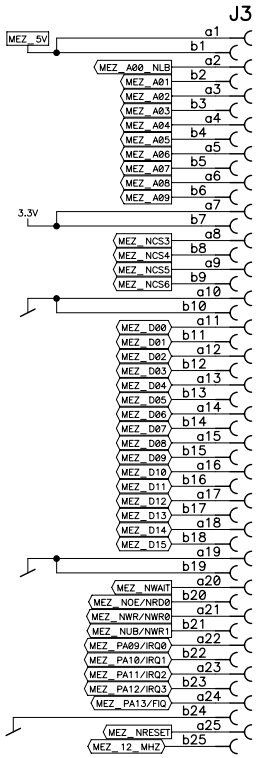
On mezzanine side

TOP SIDE



39 point-to-point IOs
+ 1 global reset
+ 1 global clock (CLOCK)

BOTTOM SIDE

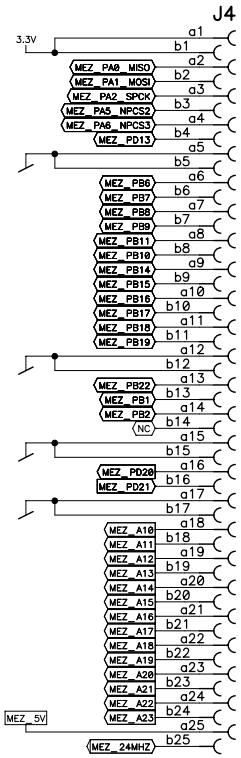


39 point-to-point IOs
+ 1 global reset
+ 1 global clock (CLOCK)

Mezza B

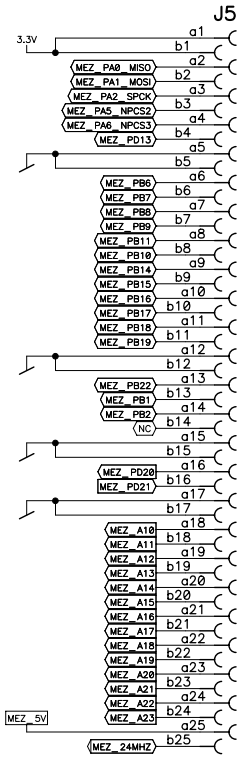
On mezzanine side

TOP SIDE



37 point-to-point IOs
+ 1 global clock (MCK0)

BOTTOM SIDE



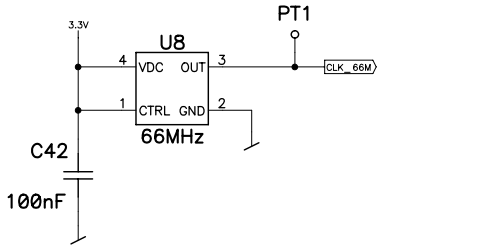
37 point-to-point IOs
+ 1 global clock (MCK0)

FPGA_EBS Part : Mezzanine		DES	02.2008 Valentini Samuel
		REV	{Revision}
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS		7/13	...\FPGA-EBS\FPGA_EBS_V1.1\FPGA_EBS_V2_0.sch

Crystal Oscillator

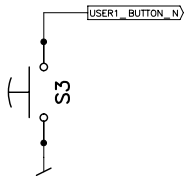
On mezzanine side

Frequency Output Test Point 66MHz



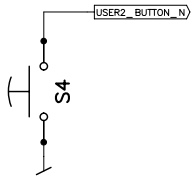
USER1 Button

On mezzanine side



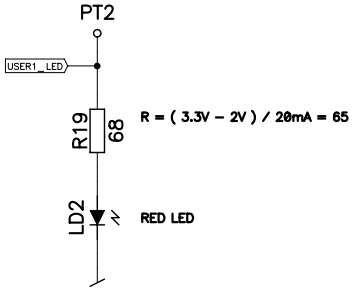
USER2 Button

On mezzanine side



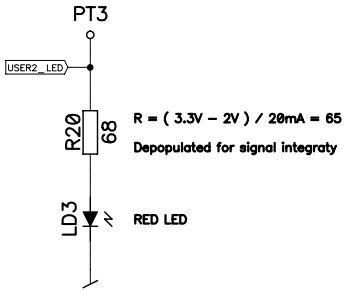
USER1 LED

On mezzanine side



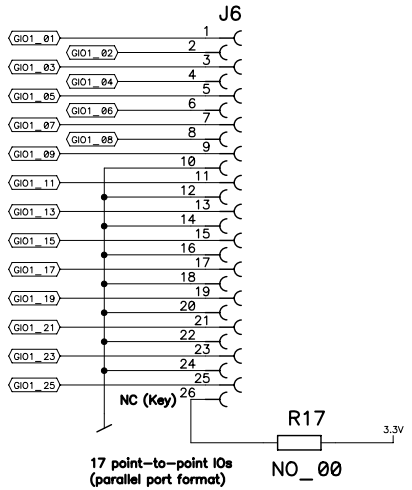
USER2 LED

On mezzanine side



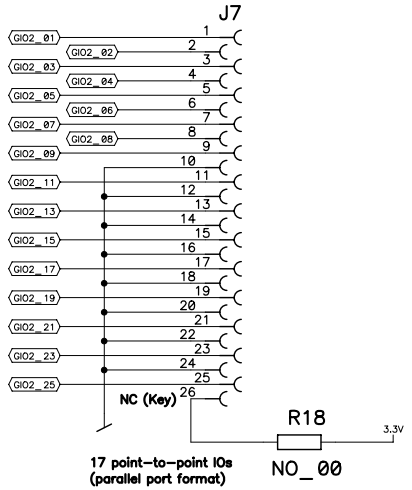
General purpose Connector

On mezzanine side



General purpose Connector

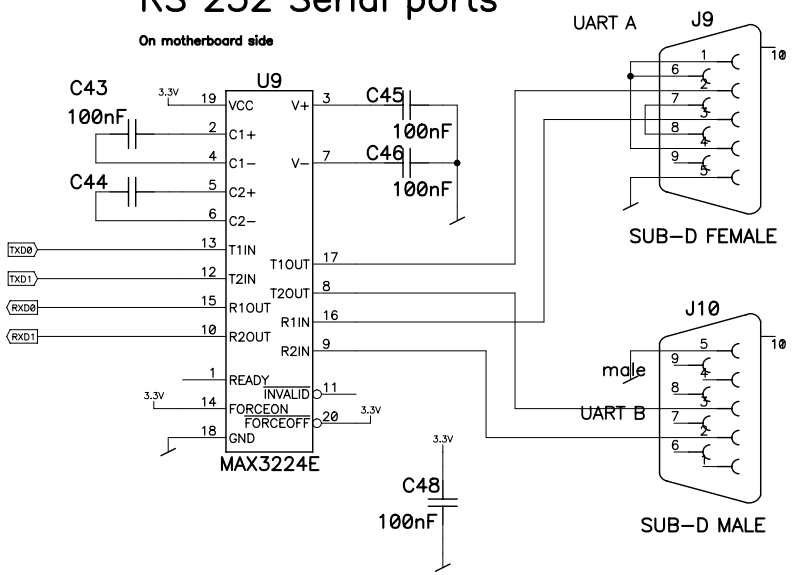
On mezzanine side



FPGA_EBS Part : Point-to-point IOs		DES	02.2008 Valentini Samuel
		REV	{Revision}
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS		8/13	...\FPGA-EBS\FPGA_EBS_V1.1 FPGA_EBS_V2_0.sch

RS 232 Serial ports

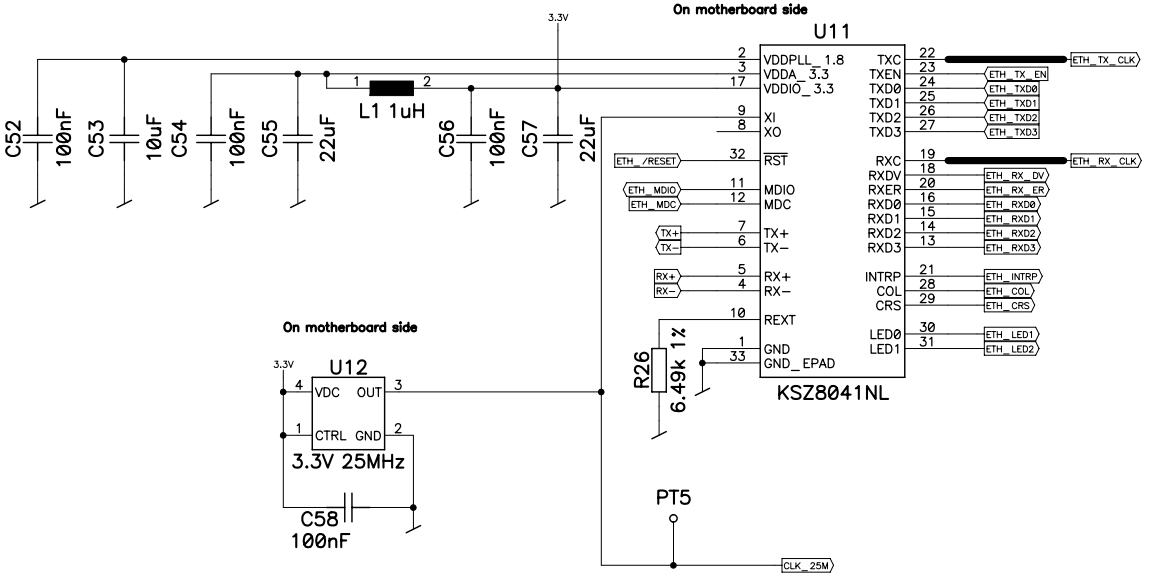
On motherboard side



Ethernet controller

TX_CLK and RX_CLK must be longer than other signals on MII.

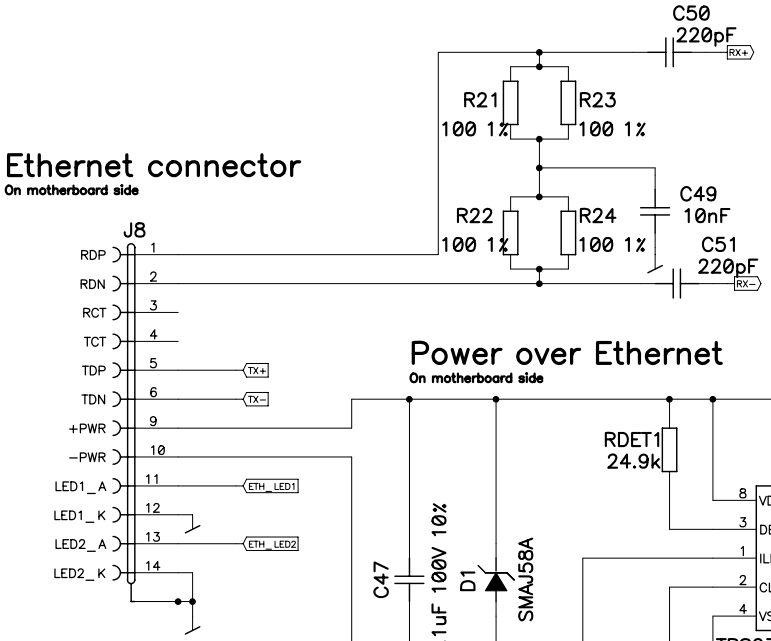
On motherboard side



On motherboard side

Ethernet connector

On motherboard side



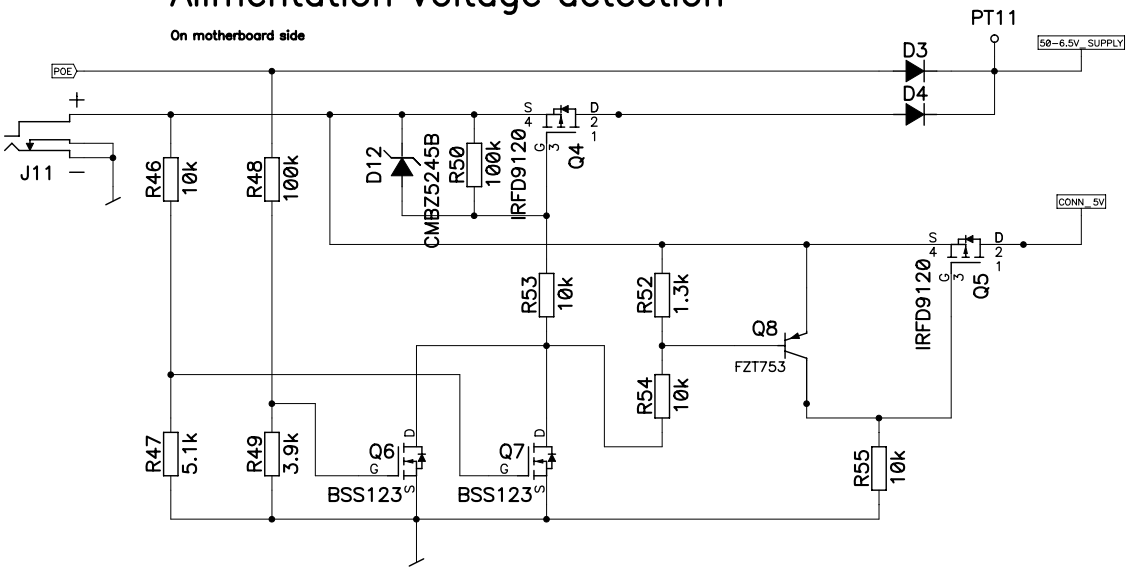
Power over Ethernet

On motherboard side

FPGA_EBS		DES	02.2008 Valentini Samuel
Part :	Ethernet / RS232	REV	{Revision}
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS		9/13	...\FPGA-EBS\FPGA_EBS_V1.1 FPGA_EBS_V2_0.sch

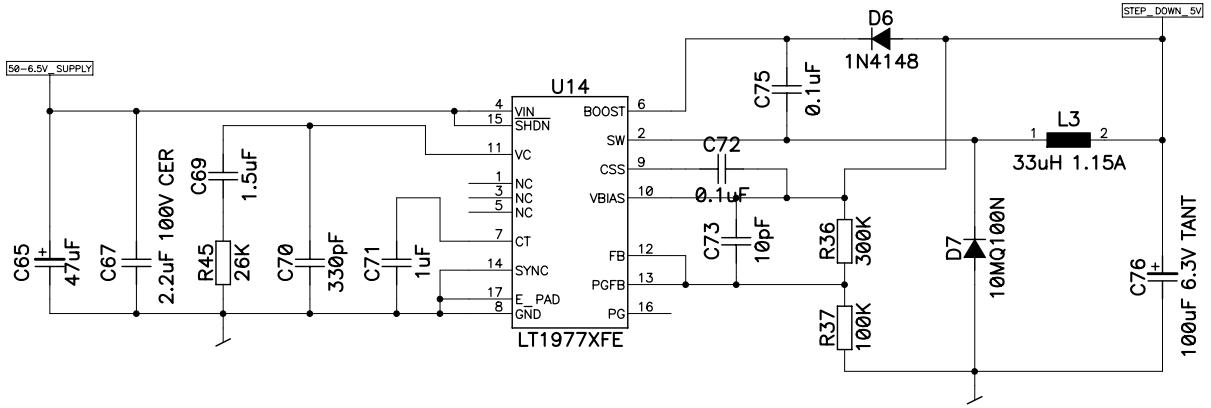
Alimentation Voltage detection

On motherboard side



Power supply 5V/1A from xV

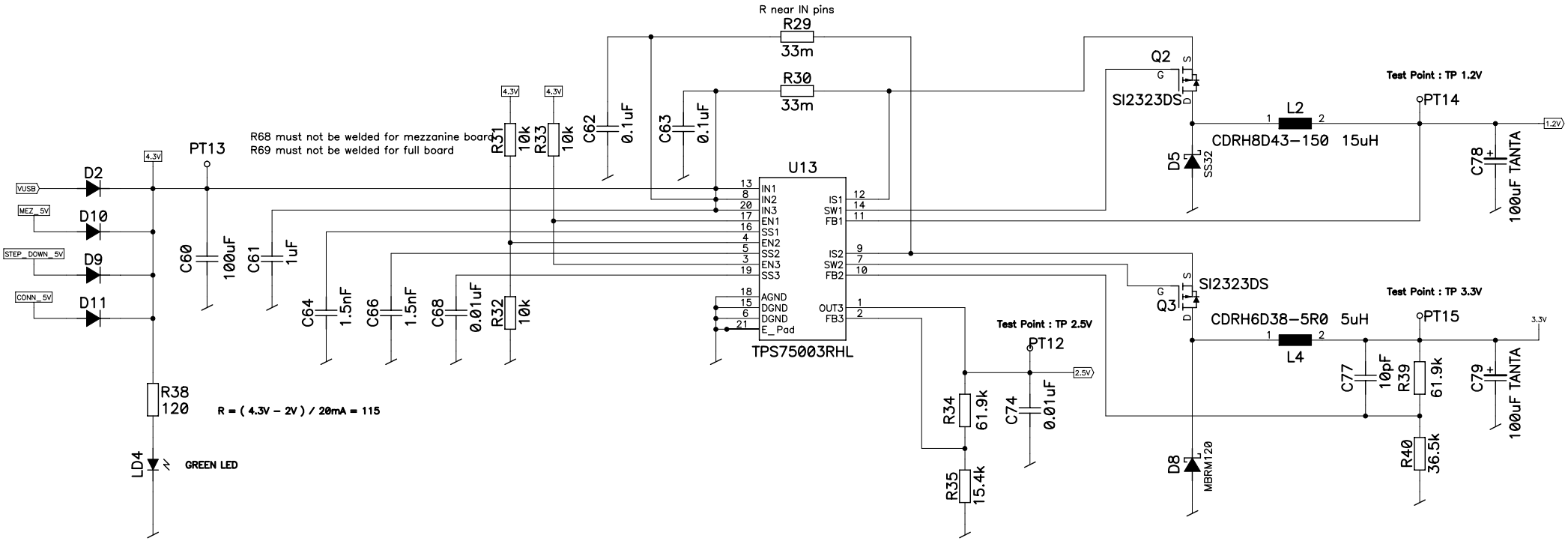
On motherboard side



FPGA_EBS		DES	02.2008 Valentini Samuel
Part :	Power 1	REV	{Revision}
HAUTE ECOLE VALAISANNE – ECOLE D'INGENIEURS		10/13	...\FPGA-EBS\FPGA_EBS_V1.1 FPGA_EBS_V2_0.sch

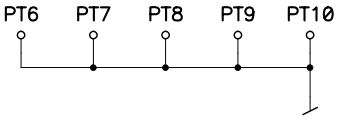
Power supply 3.3V, 2.5V and 1.2V from 4.3V

On mezzanine side



GND Test Points

All over the board



FPGA_EBS Part : Power 2		DES	02.2008 Valentini Samuel
		REV	{Revision}
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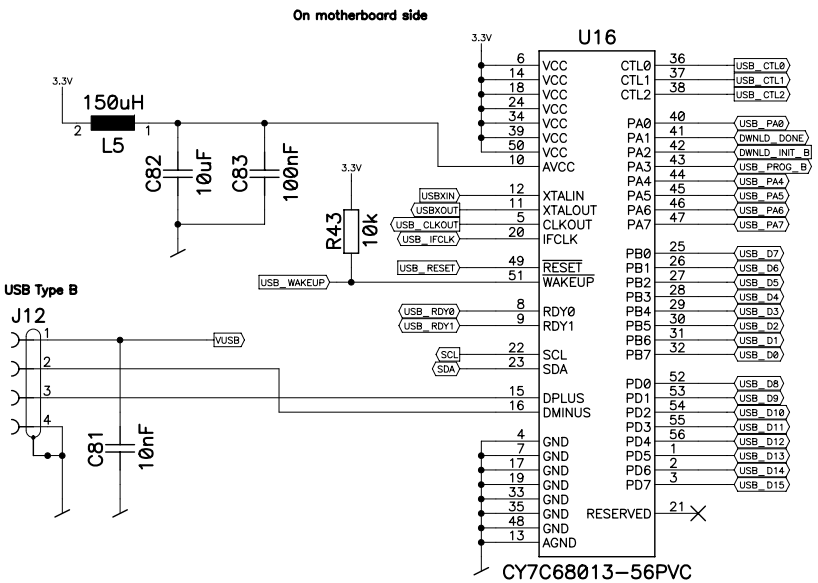
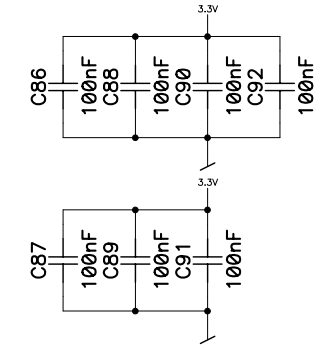
USB Controller
Cypress FX2, 8051 processor

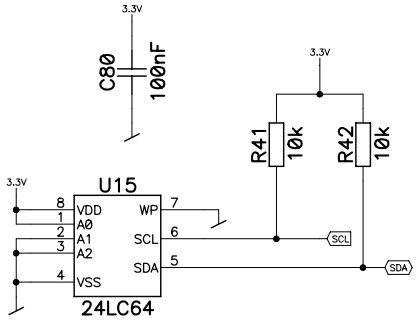
On motherboard side





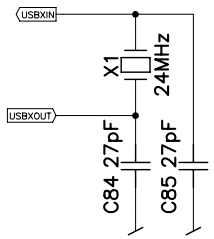
EEPROM
for USB
256 x 8

On motherboard side



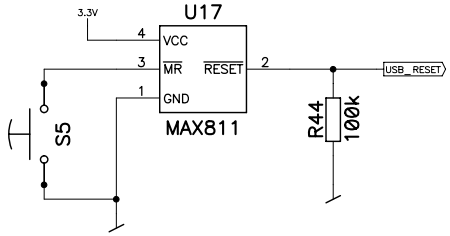
QUARTZ for USB

On motherboard side



Reset for USB

On motherboard side



FPGA_EBS		DES	02.2008 Valentini Samuel
Part :	USB	REV	{Revision}
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