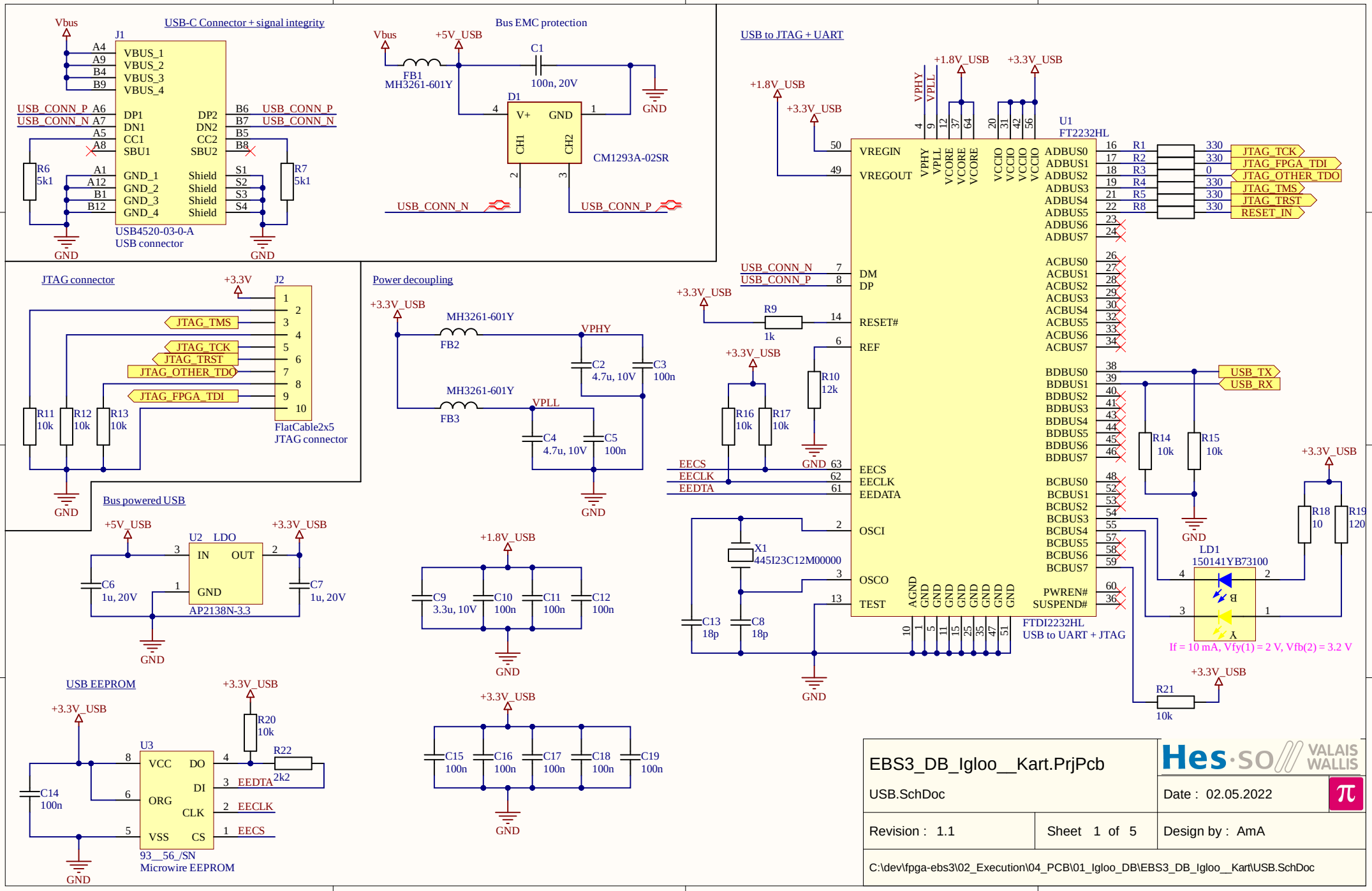

EBS3_DB_Igloo__Kart.PrjPcb	Hes·SO VALAIS WALLIS
USB.SchDoc	Date : 02.05.2022
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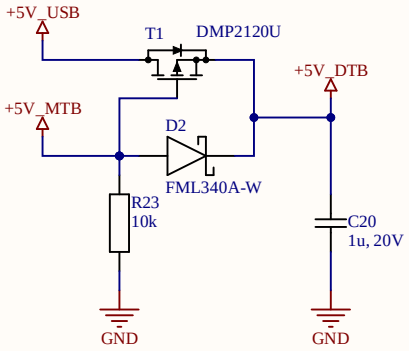
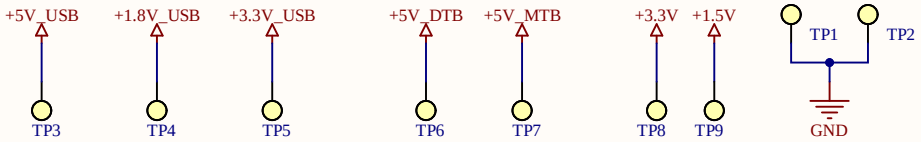
5V selector

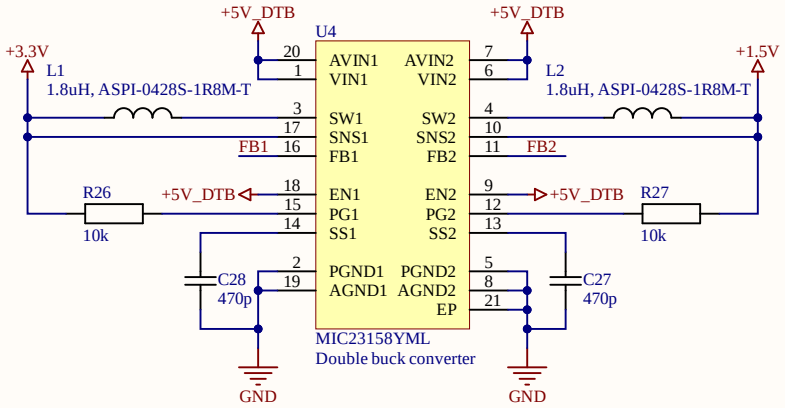


Test points

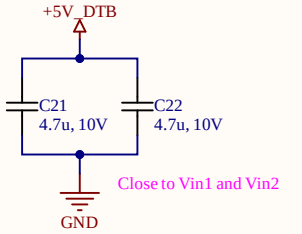


Indicate voltages on silk
Separate the GND on two points of the board

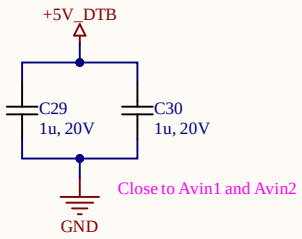
Buck converters



Keep a great connectivity with ground to dissipate heat



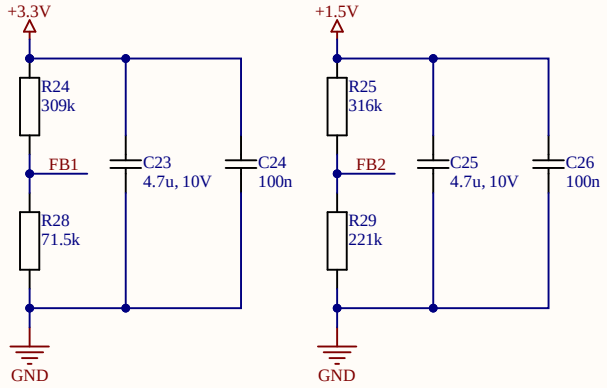
Close to Vin1 and Vin2



Close to Avin1 and Avin2

Output voltage definition

Vout = Vref (1+ Rh / Rl), with Vref = 0.62 V



EBS3_DB_Igloo__Kart.PrjPcb		Hes·so VALAIS WALLIS
Power.SchDoc		Date : 02.05.2022
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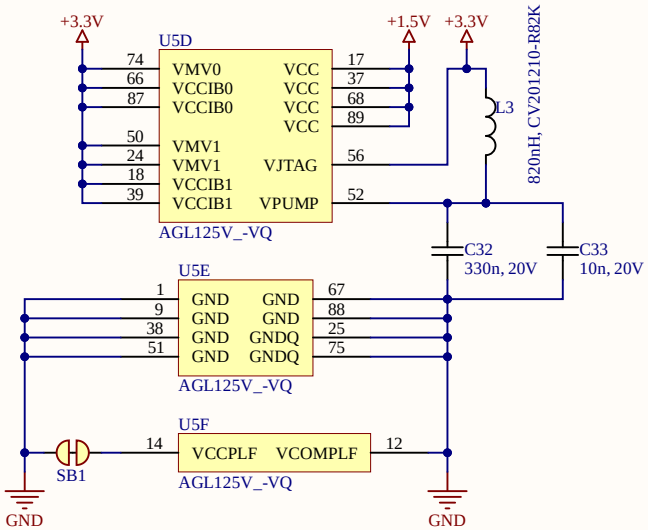
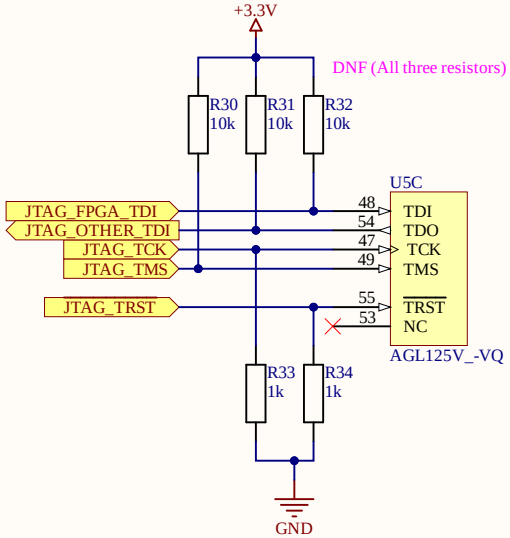
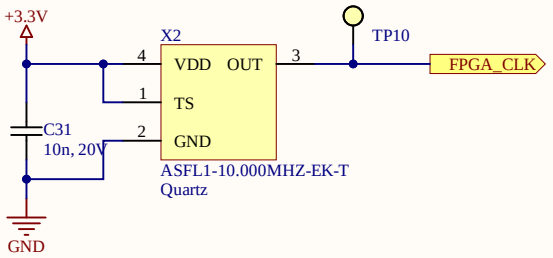
FPGA Power

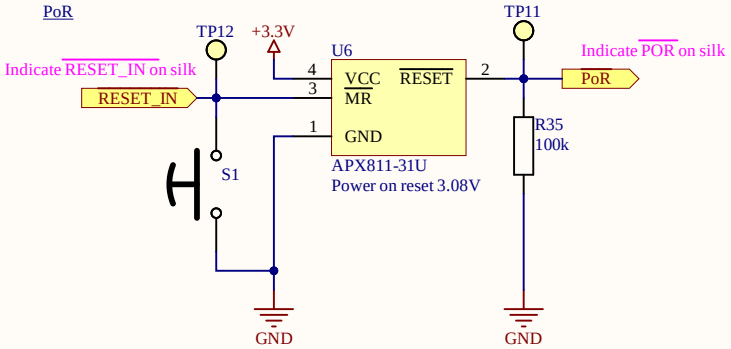




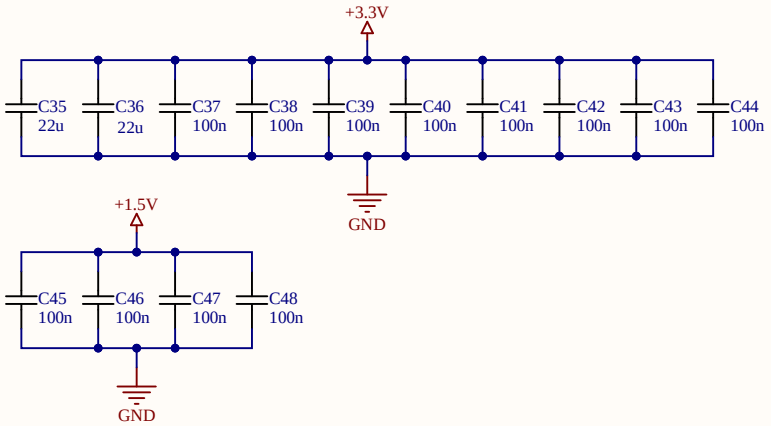
Clock



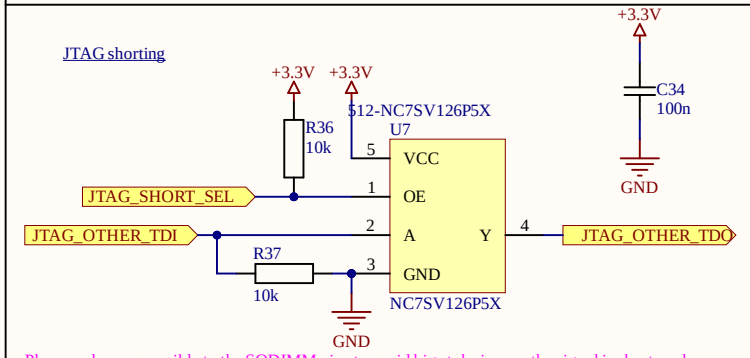
PoR



Decoupling



JTAG shorting



Place as close as possible to the SODIMM pins to avoid big stubs in case the signal is shortened

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FPGA_AlimPeriph.SchDoc		Date : 02.05.2022
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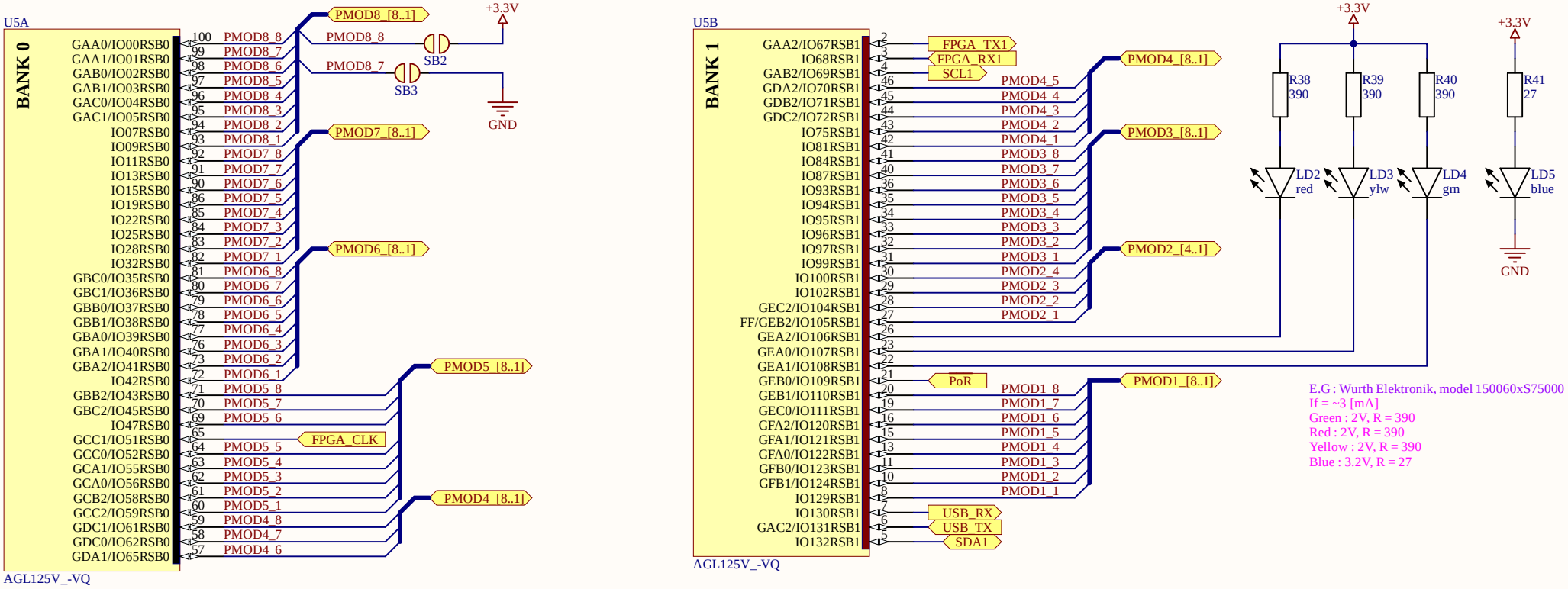
C:\dev\fpga-ebs3\02_Execution\04_PCB\01_Igloo_DB\EBS3_DB_Igloo__Kart\FPGA_AlimPeriph.SchDoc		

FPGA IOs

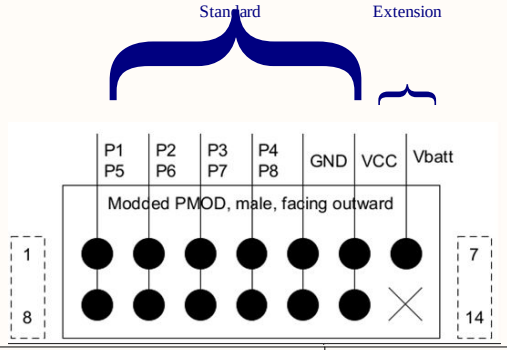
Solder bridges must be short for AGL250
Please note on silk (AGL250 : short Others : open)



E.G : Wurth Elektronik, model 150060xS75000
If = ~3 [mA]
Green : 2V, R = 390
Red : 2V, R = 390
Yellow : 2V, R = 390
Blue : 3.2V, R = 27

All pins can be switched, except CLK
Solder bridges must remain as is on pins 99 and 100
FF (pin 27) must appear on the single-row PMOD2 connector
PMOD2 should preferablly be a 90° connector

For PMODs on motherboard, indicate "standard" and "extension" on silk behind the connector such as :
Indicate related PMODx connector number (1 to 8) and, if possible, the pins Px (1 to 8)
For single-row PMOD (PMOD2), use the pins 1 to 7 (with Vbatt included)



EBS3_DB_Igloo__Kart.PrjPcb		Hes·so VALAIS WALLIS
FPGA_IO.SchDoc		Date : 02.05.2022
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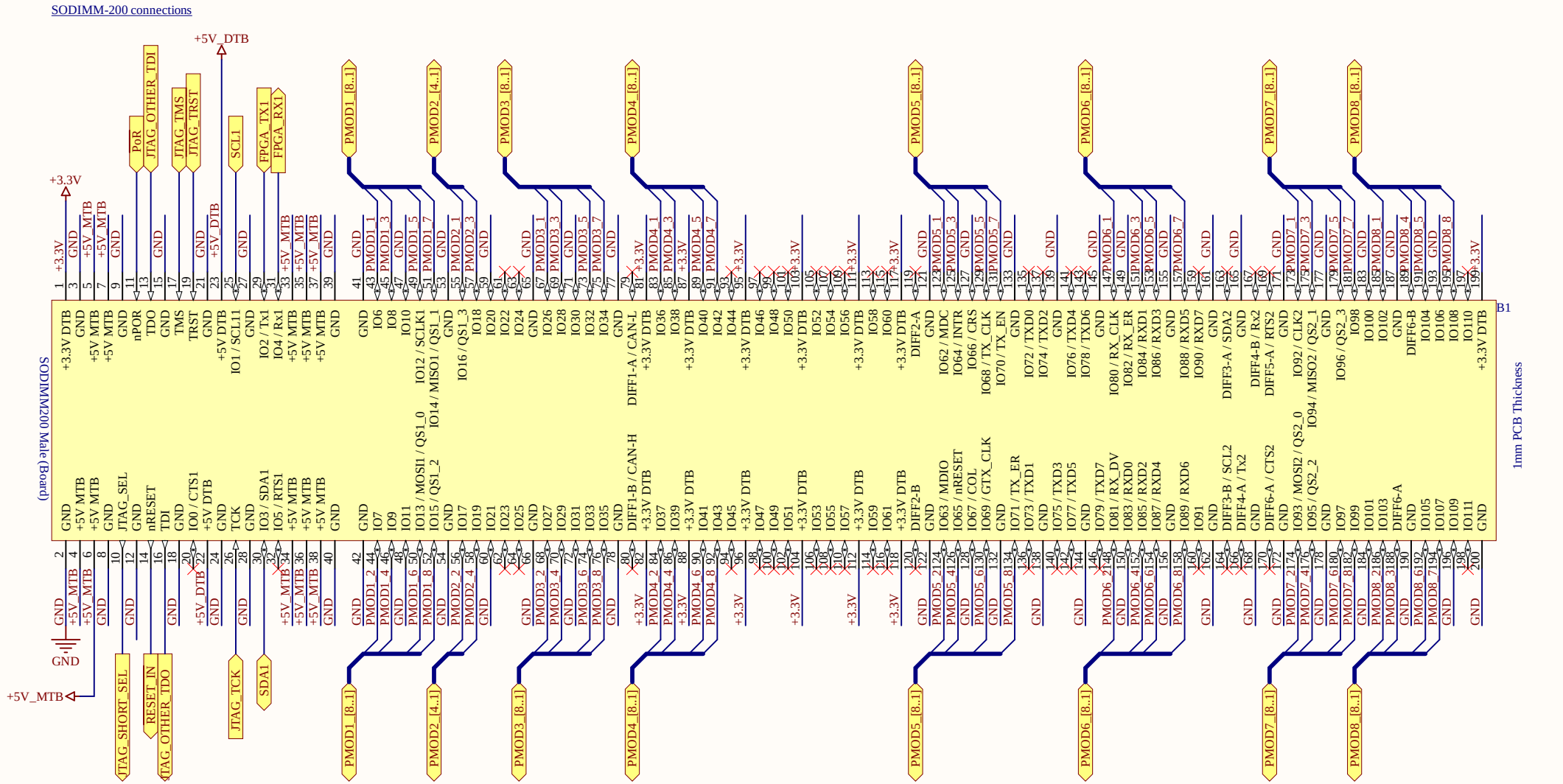

EBS3_DB_Igloo__Kart.PrjPcb		Hes·so VALAIS WALLIS
SODIMM200.SchDoc		Date : 02.05.2022
Revision : 1.1	Sheet 5 of 5	Design by : AmA
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