Annexe R

HiSADDA Core : Programmation du bitstream FPGA dans la FLASH

Redacted in english for direct integration into the HES-SO Valais UIT Wiki.

Start point

After synthesis, mapping and bitstream generation, we have a *.bit* file, usable for configure the FPGA directly by JTAG. If we want to put it into the boot FLASH, the following steps can be followed.

Generating the PROM file

Click on "*Create PROM File (PROM File Formatter)*".

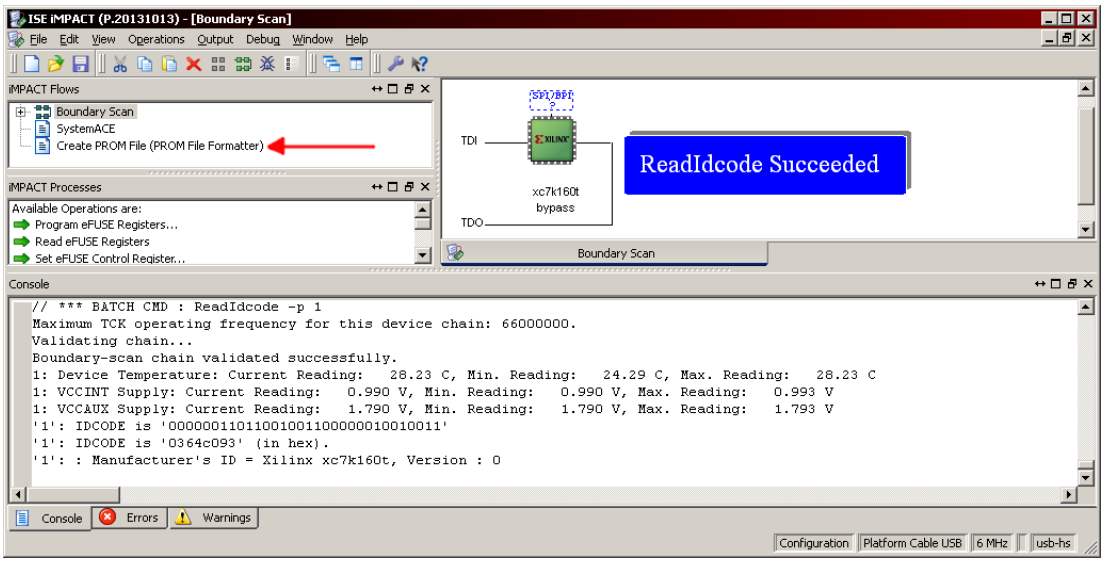

FIGURE R.1 – Xilinx iMPACT : Create PROM File

The following dialog will appears. Configure all fields like the next figure. Set the name and the path according to your needs.

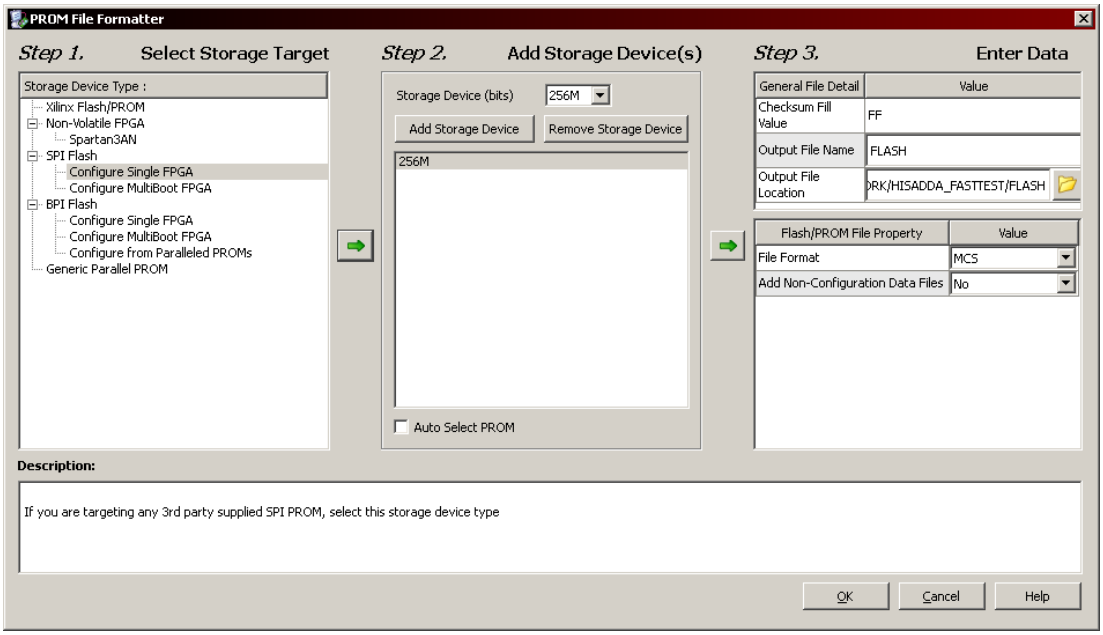

FIGURE R.2 – Xilinx iMPACT : PROM File Formatter

The next dialog will follows. Add first your *.bit* bitstream ("Add Xilinx Device...") and the then generate the PROM file ("Generate File...").

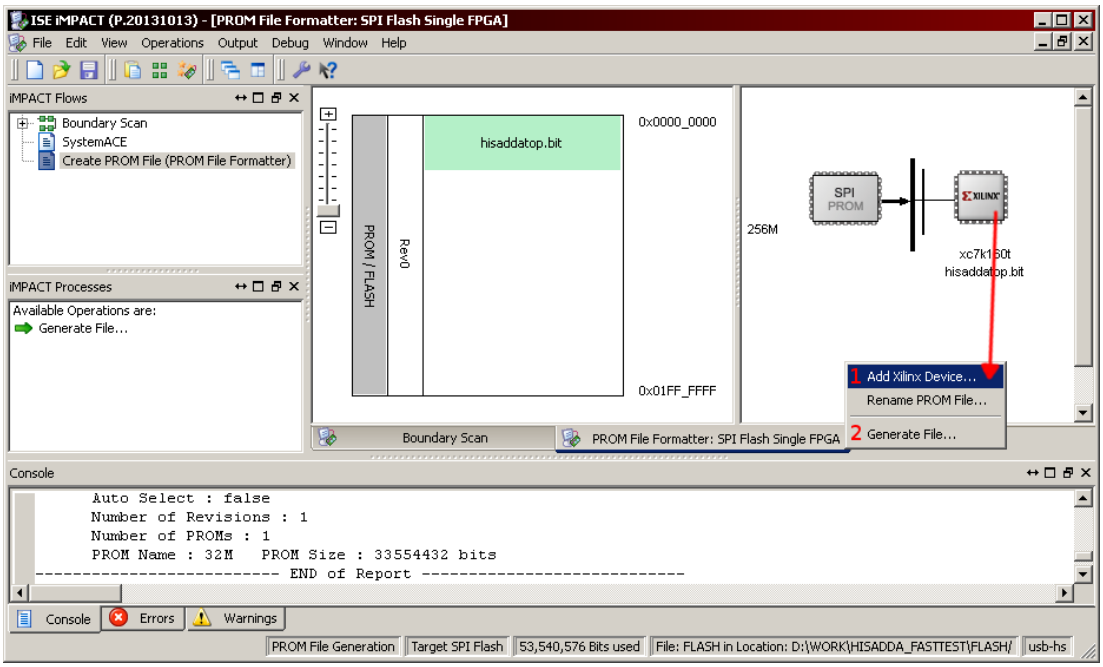

FIGURE R.3 – Xilinx iMPACT : Create PROM File

Come back to the JTAG boundary scan view, right click on the FPGA and "Select Attached SPI/BPI". In the dialog, set the values like this screenshot - or adapt it if you have soldered another smaller/bigger/-compatible serial FLASH device.

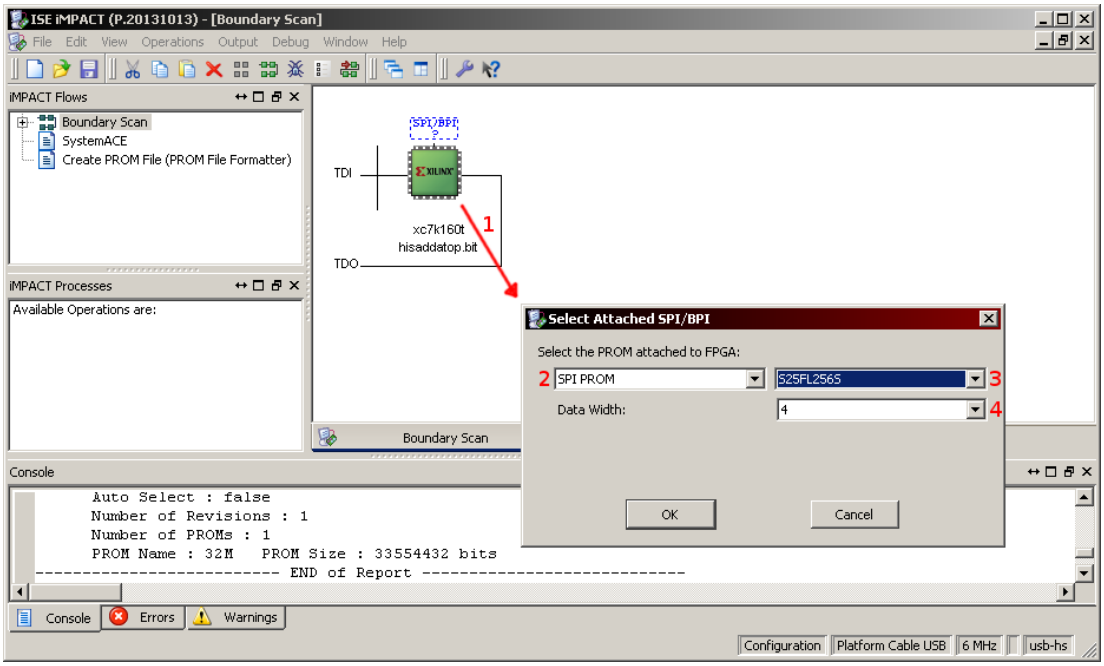

FIGURE R.4 – Xilinx iMPACT : Select Attached SPI/BPI

Now, the FLASH is visible and attached to the FPGA.

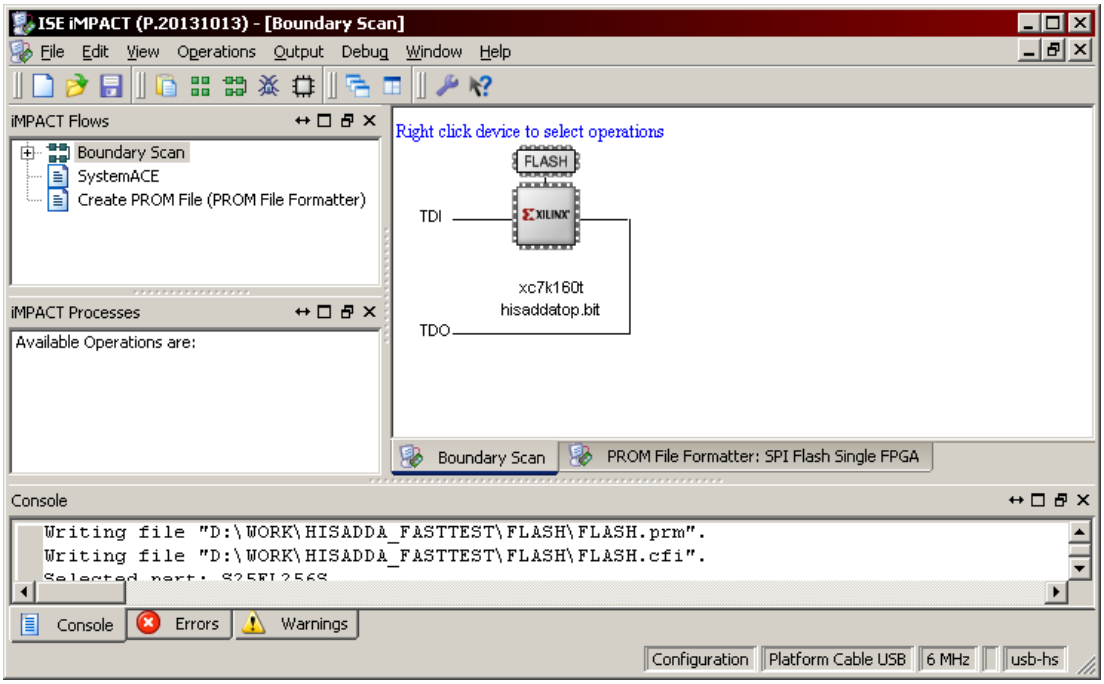

FIGURE R.5 – Xilinx iMPACT : FLASH attached to FPGA

Finally, you can program the FLASH [72] : ...and be patient : the operation lasts about 1 hour !

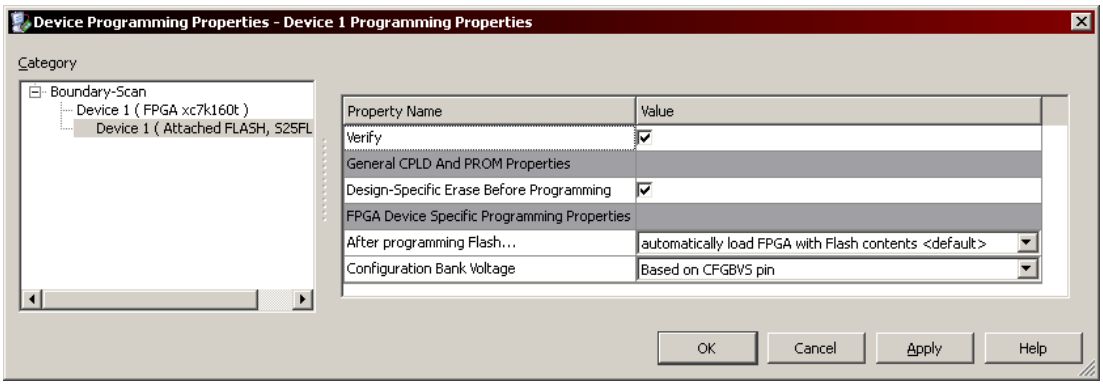

FIGURE R.6 – Xilinx iMPACT : Device Programming

72. Be extremely careful to not change the "Configuration Bank Voltage" to "Low", otherwise severe hardware damages on the DDR3 SDRAM will occur. Leave this parameter to "Based on CFGBVS pin".