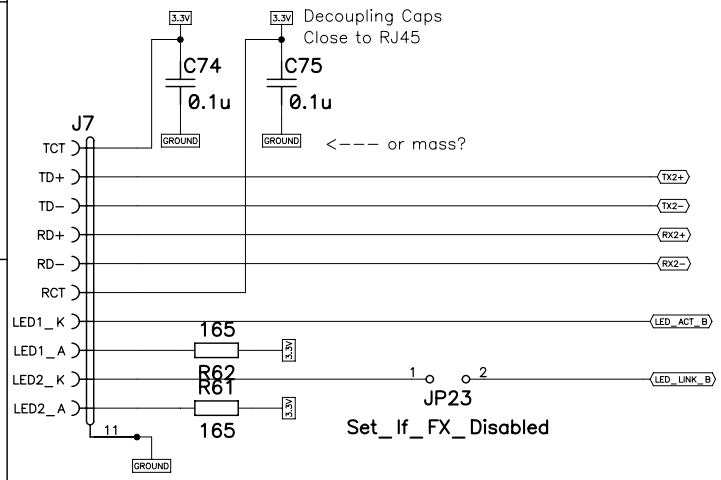
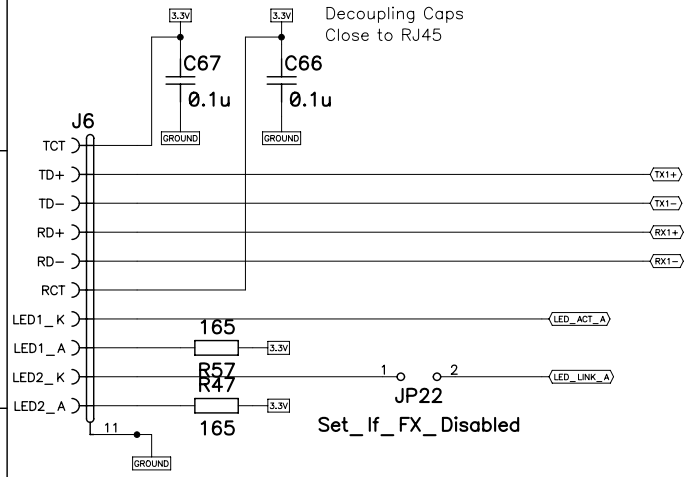
INDEX OF PAGES FOR THE INTERFACE (RJ45 and Optical)

NUMBER	NAME	DESCRIPTION	COMMENTS
1	Index	Description of sheets	This is this page
2	Ethernet Input	Input connectors	Contains the RJ45–plugs and fiber–plugs
3	Input switching	Input switching from RJ45 to Optical	This is the Jumper page to switch fiber<–>RJ45 ...
4	Buffer / PHY	High Impedace Buffer and PHY	Contains the Ethernet Phy
5	CPLD Connector	CPLD and Connector 3*32 Pin	Contains the connection to other board and the CPLD
6	Power Supply	Power Supply Parts	Contains the power parts 5V, 3,3V
7	Divers	Clock, JTAG, RS422	Contains Clock generation, JTag, RS422 and Board Reset

Ethernet RJ45 input

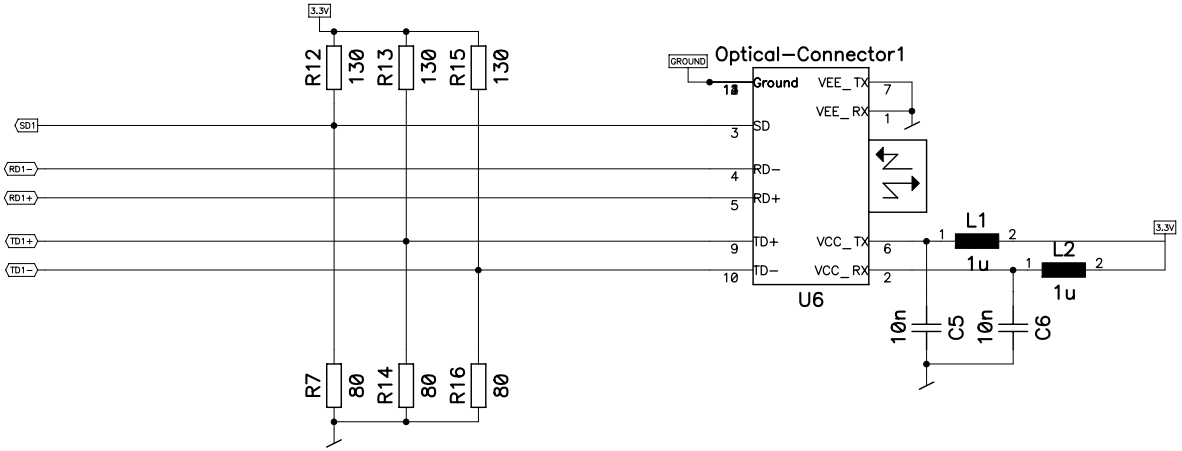
1 == Port A
2 == Port B
Caution, all blue lines should have a line impedance of 100/50 Ohm.

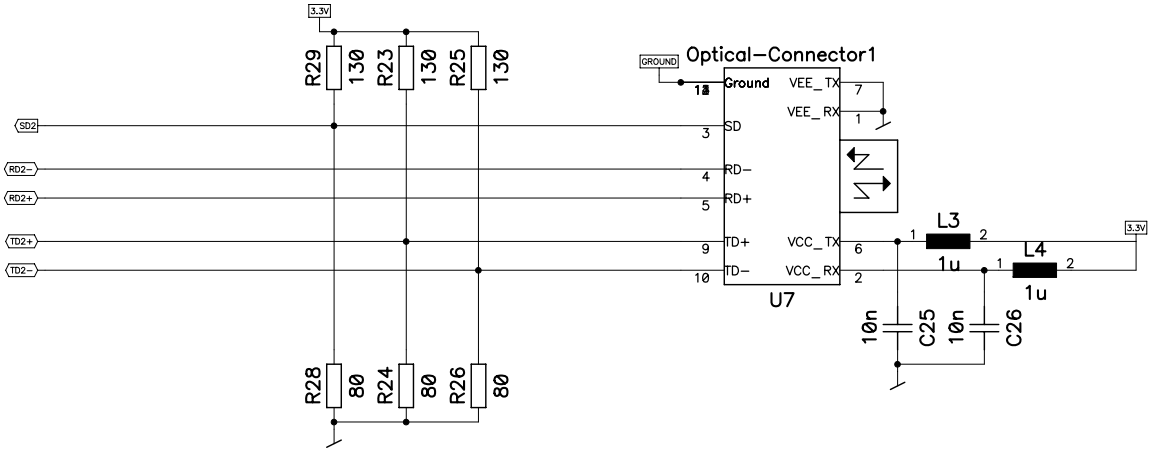




Ethernet optical fiber input

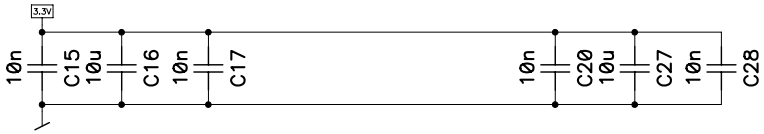
Optical fiber input
Caution, all Capacitors and Resistances close to the Connectors





Decoupling caps

The decoupling capacitors are placed on the bottom layer and close to the fiber-plug's --->



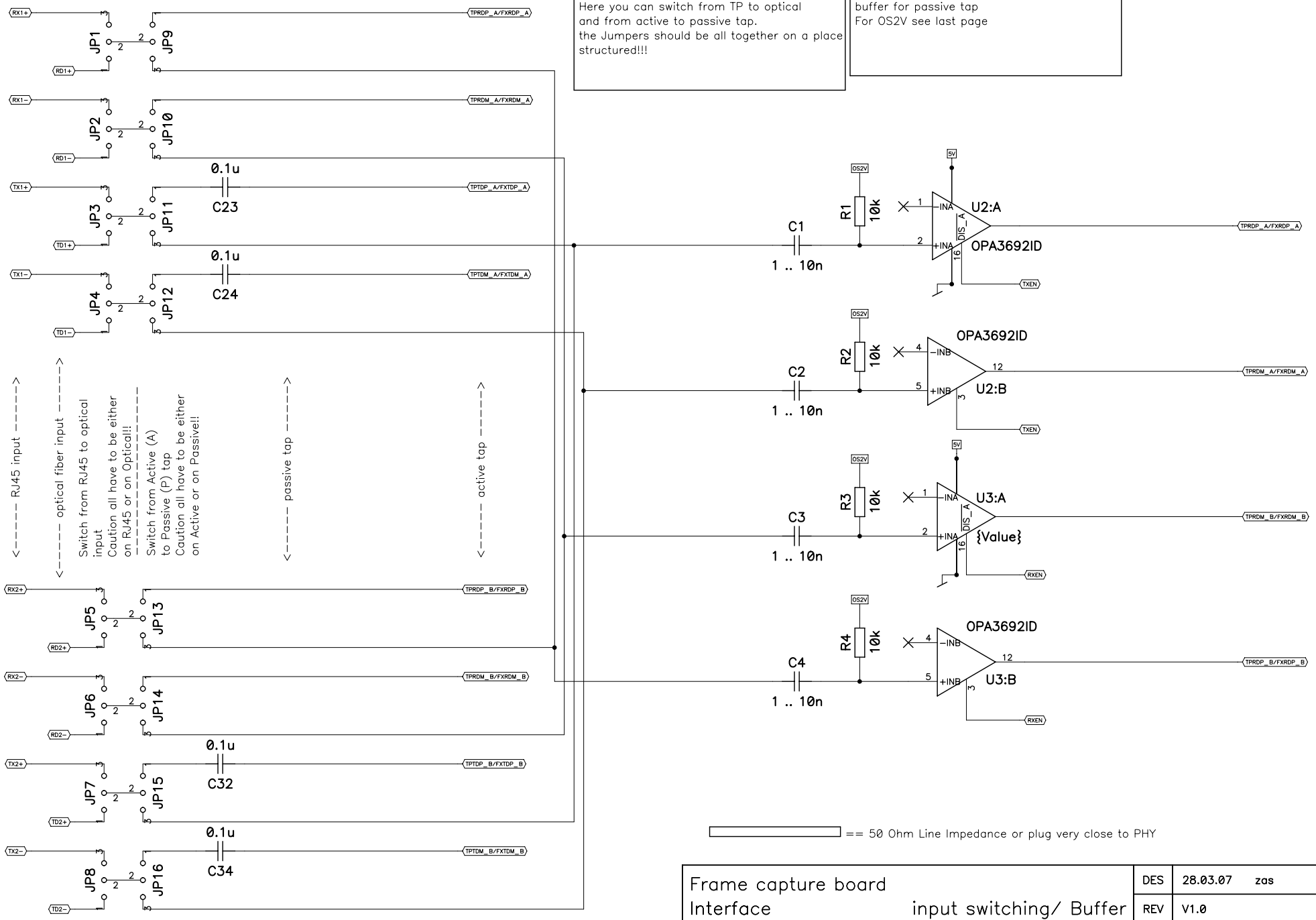
Frame capture board Interface — Ethernet Input	DES	28.03.07 zas
	REV	V1.0
HAUTE ECOLE VALAISANNE	2/7	{Path} Interface.sch

Ethernet input switching

Here you can switch from TP to optical
and from active to passive tap.
the Jumpers should be all together on a place
structured!!!

High impedance buffer

buffer for passive tap
For OS2V see last page



== 50 Ohm Line Impedance or plug very close to PHY

Frame capture board Interface input switching/ Buffer	DES	28.03.07 zas
	REV	V1.0
HAUTE ECOLE VALAISANNE	3/7	{Path} Interface.sch

Ethernet transceiver (PHY)

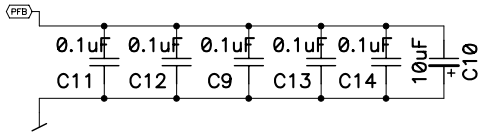
TX_CLK_A & B and RX_CLK_A & B must be longer than other signals on MII and routing of the 25MHz line is critical.

Phy Matching Network

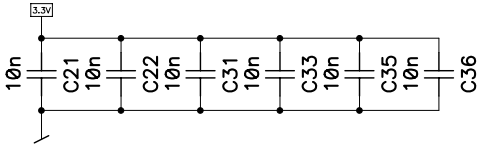
This resistors should be close to the PHY

Power Feedback Circuit

Countion these Caps should be placed close to the correspond Phy Pin (PFOUT, PFB), see Datasheet p15 & 38



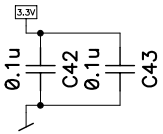
Decoupling caps for PHY, please control!!!



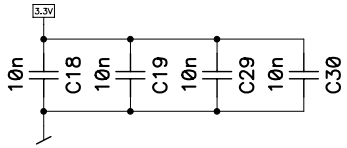
Decoupling caps

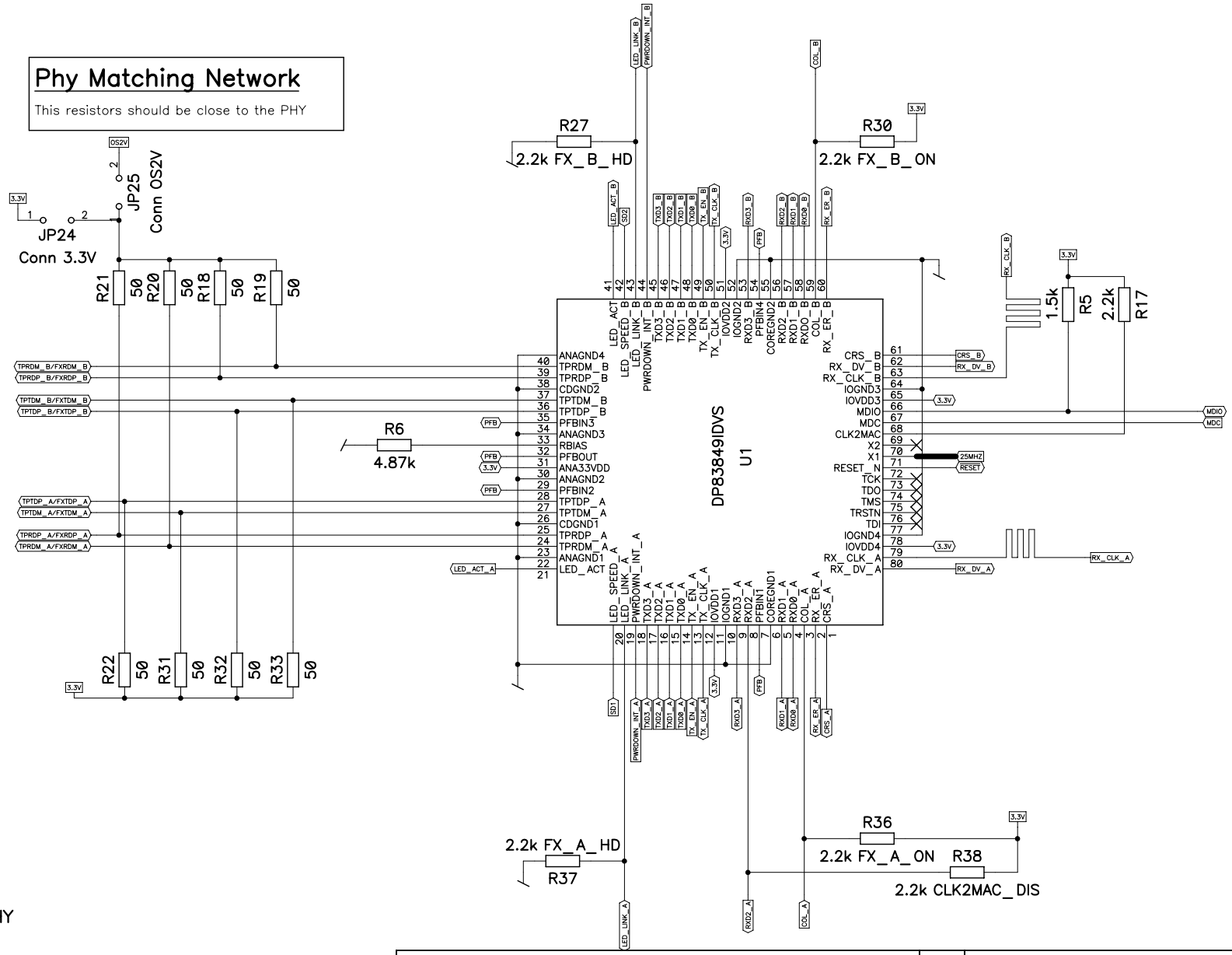
The decoupling capacitors are placed on the bottom layer. Close to Phy

For RJ45, close to PHY



For fiber, close to PHY



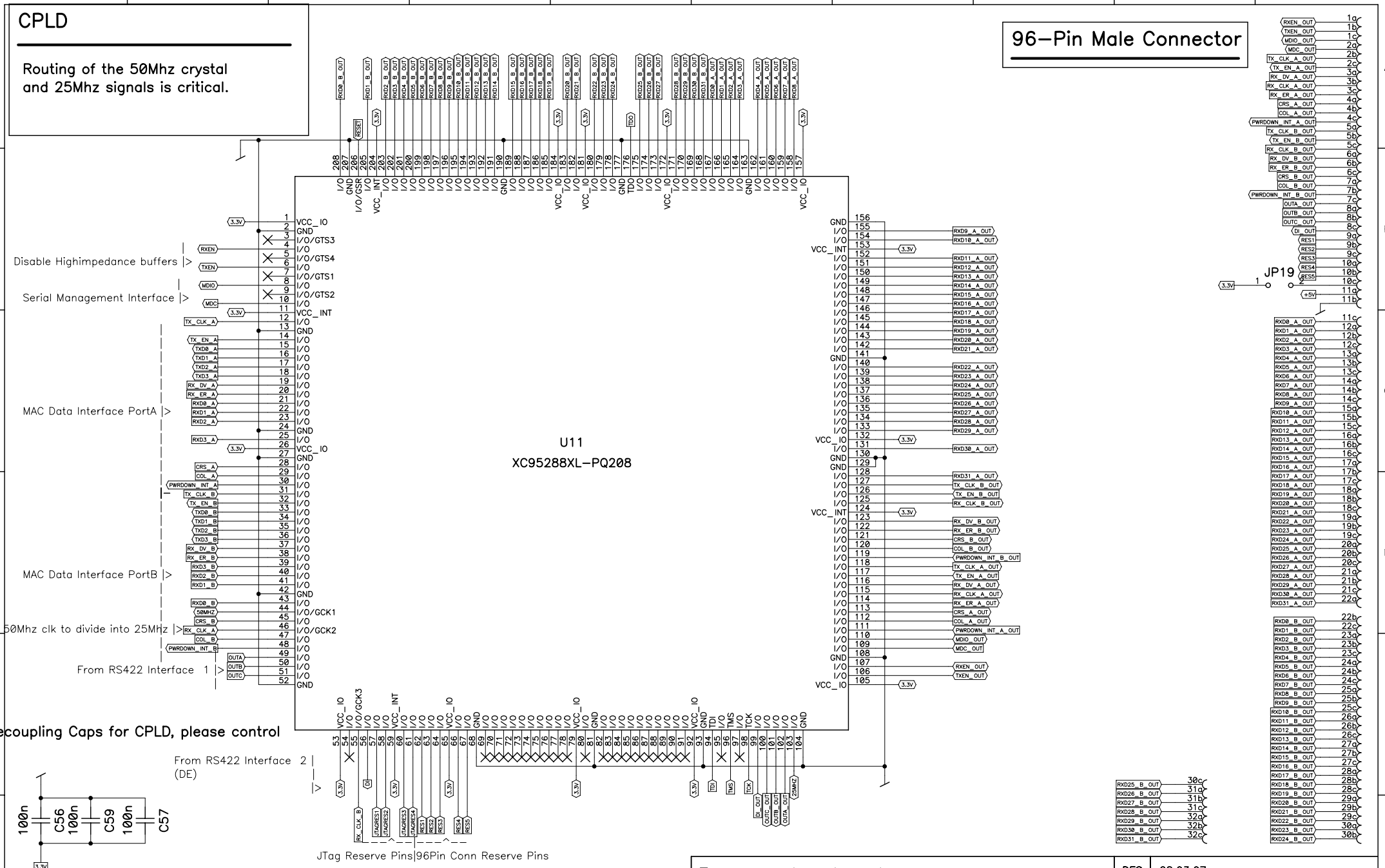


Frame capture board Interface	PHY	DES	28.03.07 zas
		REV	V1.0
HAUTE ECOLE VALAISANNE		4/7	{Path} Interface.sch

CPLD

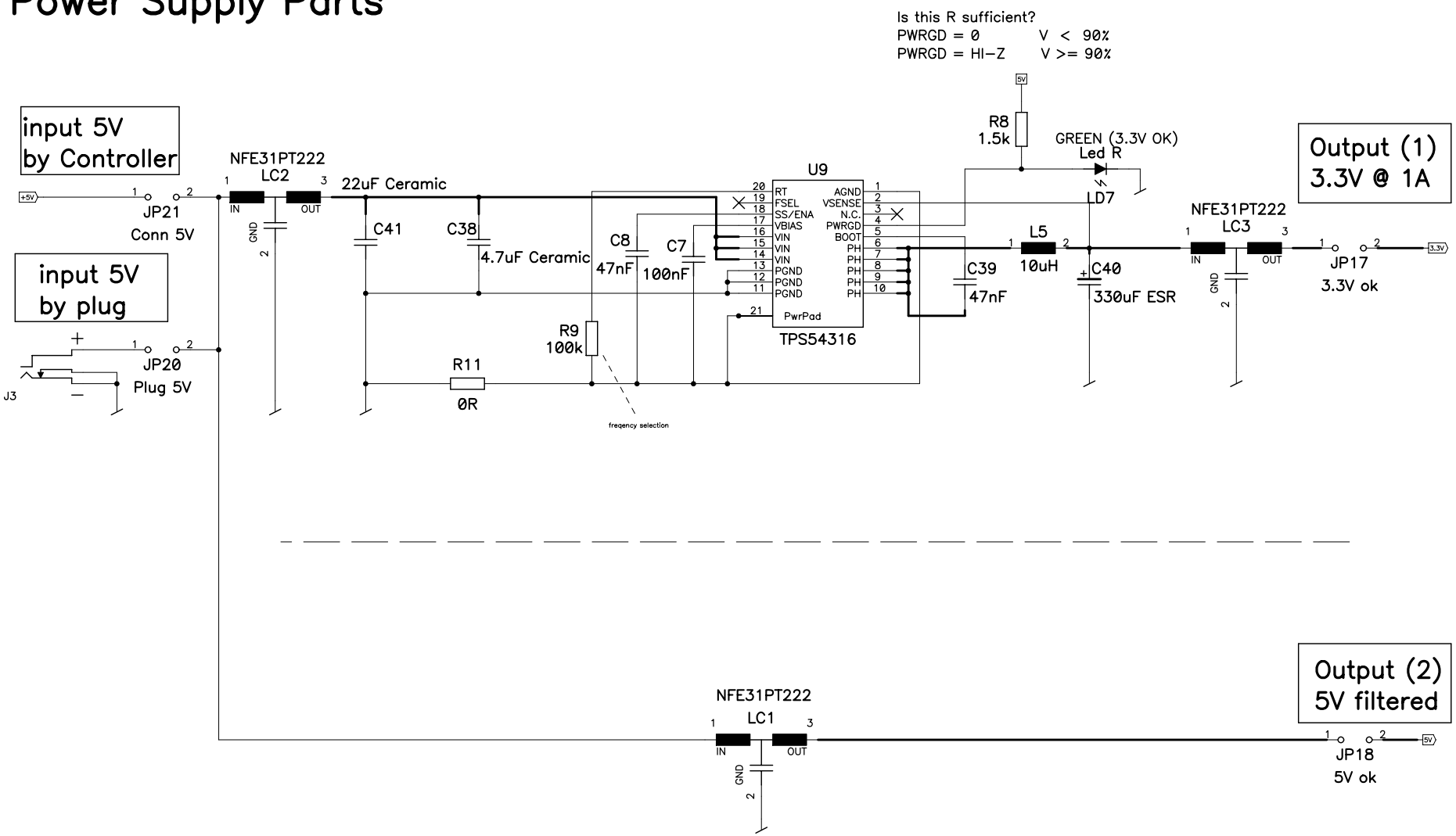
Routing of the 50Mhz crystal and 25Mhz signals is critical.

96-Pin Male Connector



Frame capture board Interface CPLD/Connector3*32	DES	28.03.07 zas
	REV	V1.0
HAUTE ECOLE VALAISANNE	5/7	{Path} Interface.sch

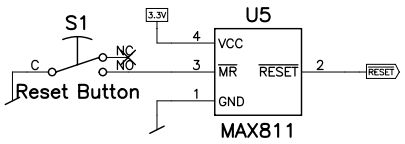
Power Supply Parts



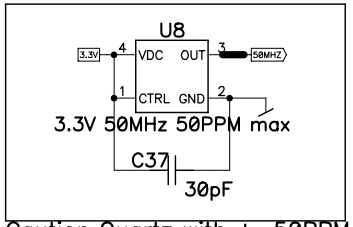
Frame capture board Interface	Power supply	DES	28.03.07 zas
		REV	V1.0
HAUTE ECOLE VALAISANNE		6/7	{Path} Interface.sch

Board reset

This IC is NOT decoupled by a capacitor, to detect small power fault.
The reset button resets the board and the JTAG.



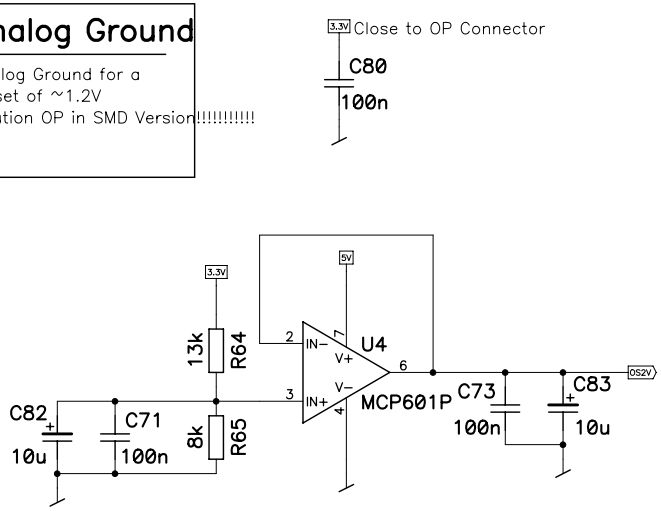
Phy clk



Caution Quartz with +−50PPM,

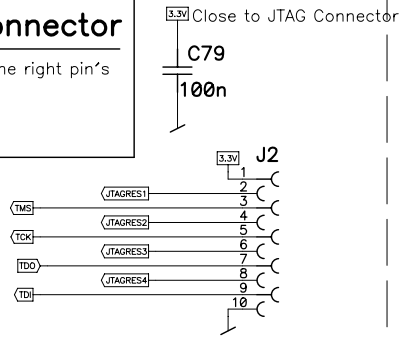
Analog Ground

Analog Ground for a offset of ~1.2V
Caution OP in SMD Version!!!!!!!!!!!

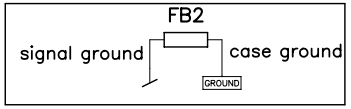


JTAG Connector

Caution, are the right pin's connected???

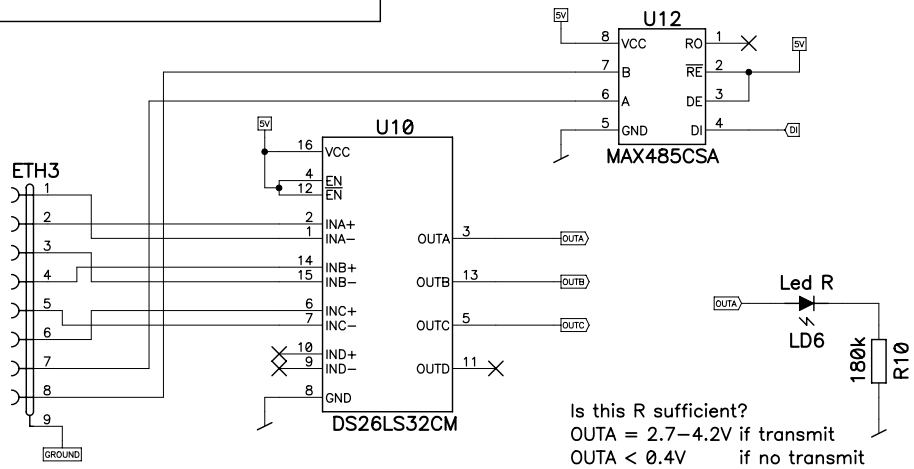


Ground



RS422 Client bloc

The led shows the transmit and receive actions.
Normal: 1−2 Port C; 3−4 Port D; 5−6 Port A
Done: 1−2 Port A; 3−4 Port B; 5−6 Port C



Is this R sufficient?
OUTA = 2.7−4.2V if transmit
OUTA < 0.4V if no transmit

Frame capture board Interface Divers	DES	28.03.07 zas
	REV	V1.0
HAUTE ECOLE VALAISANNE	7/7	{Path} Interface.sch