MOLIS / IGOR3: AD/DA Converter Board

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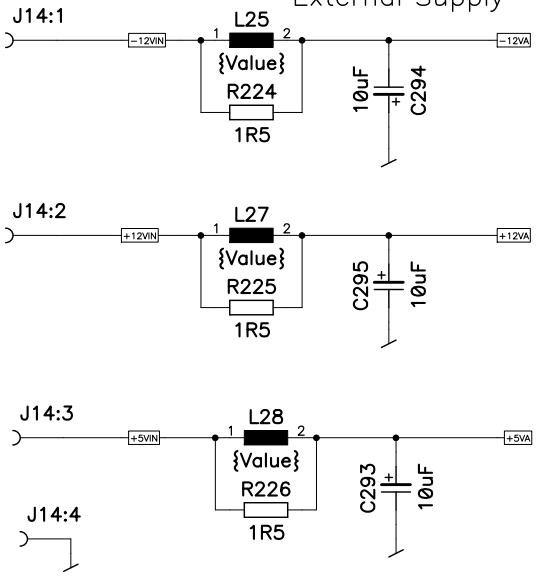
Versioning

Version	Date	Description
1.0	23. August 2011	Initial version − first issue
1.1	8. February 2012	Bugfixes / Changes: − The +2.5VA is now supplied from the +5VA instead of VEXTfor less power dissipation (Therefore the +2.5VA is no more relevant for the supply delaying) − R4 and R6 are now 1kOhm instead of 100kOhm (More drive current for the delay−chip) − C16 and C17 are now 4.7nF instead of 1nF (Delay time adaption to 4.835ms) − C134 and C137 are now 10pF instead of 5.6pF (Otherwise a special frequency response is present on the output of the DA AD5547) − There is now only one clock buffer for the MCLK for both AD7760 otherwise it doesn't work − The clock buffer for the MCLK of the AD7760 is now supplied by +2.5VD and no more +5VD because of the signal levels from the FPGA − The 100nF output capacitor of the Vocm buffer was replaced by a 100pF in series with a 100Ohm resistors to prevent oscillations which where createt with only a 100nF capacitor − The connections for the buffer of the AD7760 had to be corrected as it's stated in the datasheet − The net +5VA_AD7626 for the supply for the AD7626 was not connected to the +5VA and is now replaced by the net +5VA
2.0	22. October 2012	Bugfixes / Changes: − Integration of a Spartan−6 FPGA for A/D−D/A controll − Integration of a 3x32 pins VME compatible connector − Removal of the mezzanine connector − The +12VA, −12VA and +5VA are now directly available from the VME connecor, through the backplane − Addition of the +3.3VD and +1.2VD regulators for FPGA powering − Removal of LVDS routing bugs on the FPGA − Addition of digital line filters on the VME connector − Addition of separated data buses and command signals for each A/D−D/A − Use of Xilinx XCF32P and XCF08P as FPGA configuration memory

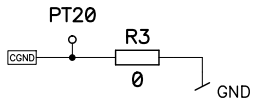
Power Supply 1

+12VA, −12VA and +5VA come directly from VME connector
and are powered by the VME rack

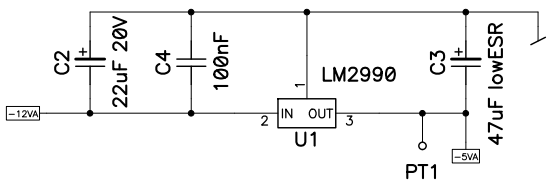
External Supply



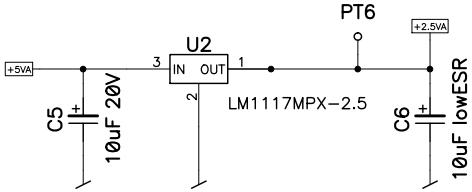
Ground bridge

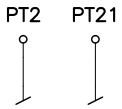


−5V Analog



+2.5V Analog



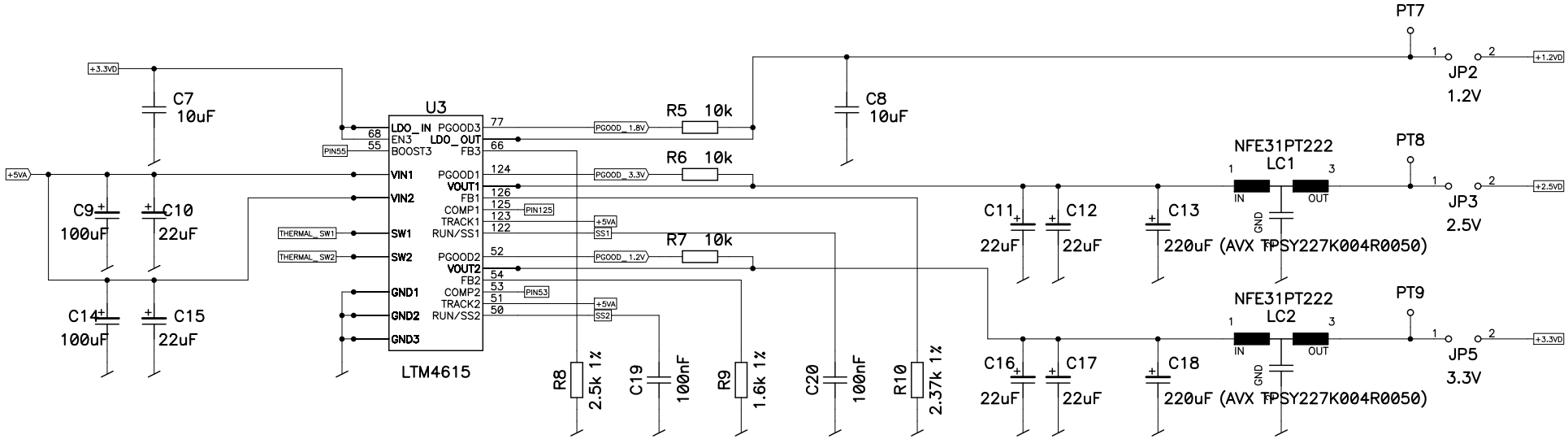


ADC / DAC Board Molis & IGOR III — Supply 1	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	2/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

Power Supply 2

LDO_OUT:
VLDO_OUT = 0.4 * (4.99k + RFBLDO) / RFBLDO
VLDO_OUT = 1.2V => RFBLDO = 2.5 kOhms
VOUT:
VOUT = 0.8 * (4.99k + RFB) / RFB
VOUT1 = 2.5V => RFB1 = 2.35 kOhms => 2.37 kOhms
=> VOUT1_REAL = 2.48 V
VOUT2 = 3.3V => RFB2 = 1.6 kOhms

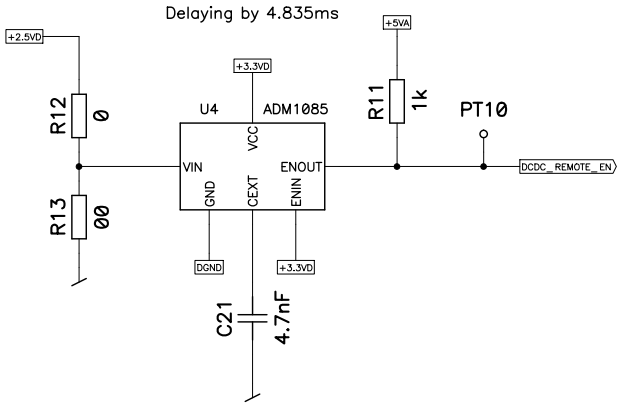
3.3V @ 4A / 2.5V @ 4A / 1.2V @ 1.5A



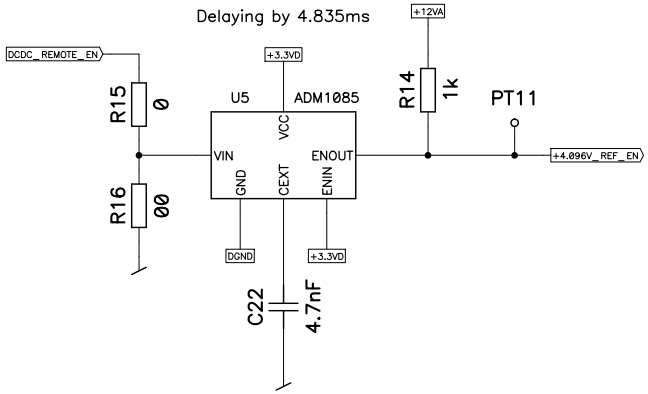
ADC / DAC Board Molis & IGOR III — Supply 2	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	3/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

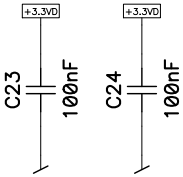
Supply Delaying

Supply Delaying (AD7626)



Reference Delaying (AD7626)

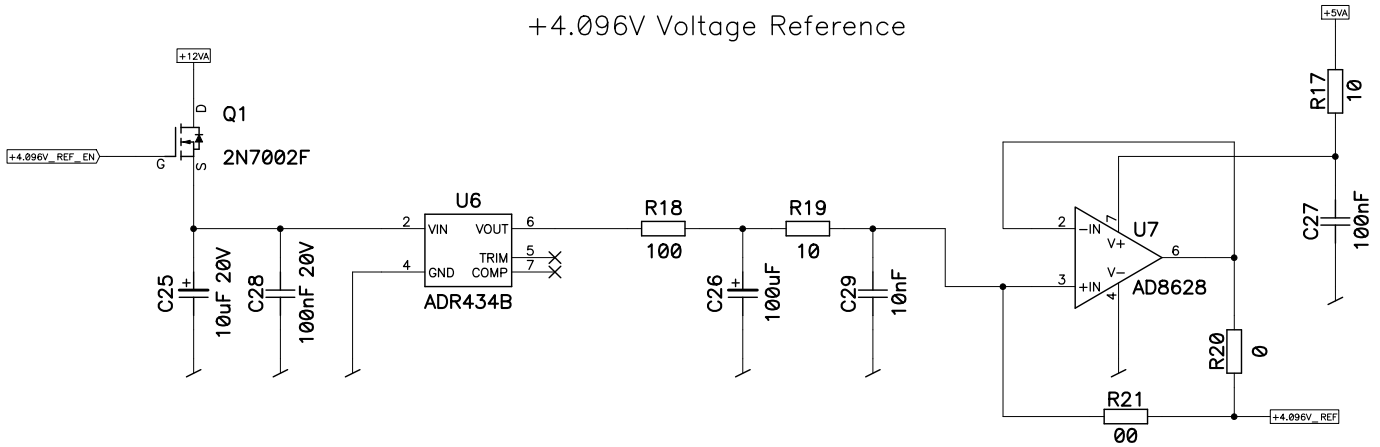




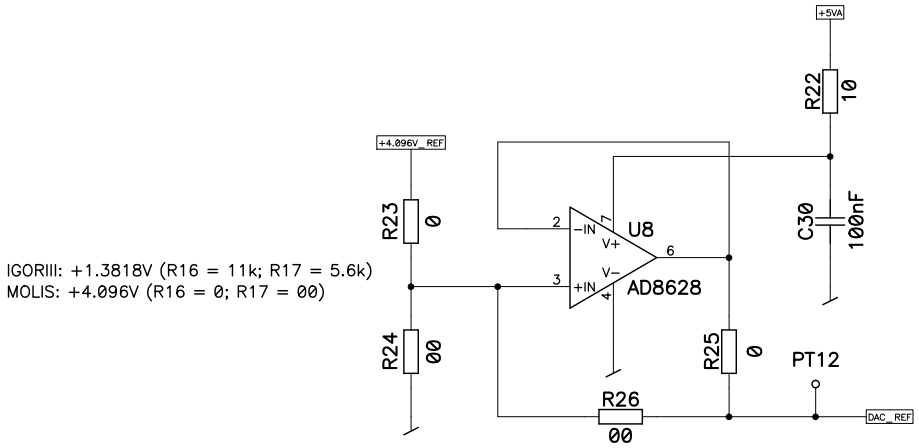
ADC / DAC Board Molis & IGOR III — Supply Delaying	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	4/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

Voltage Reference

+4.096V Voltage Reference



DAC Voltage Reference

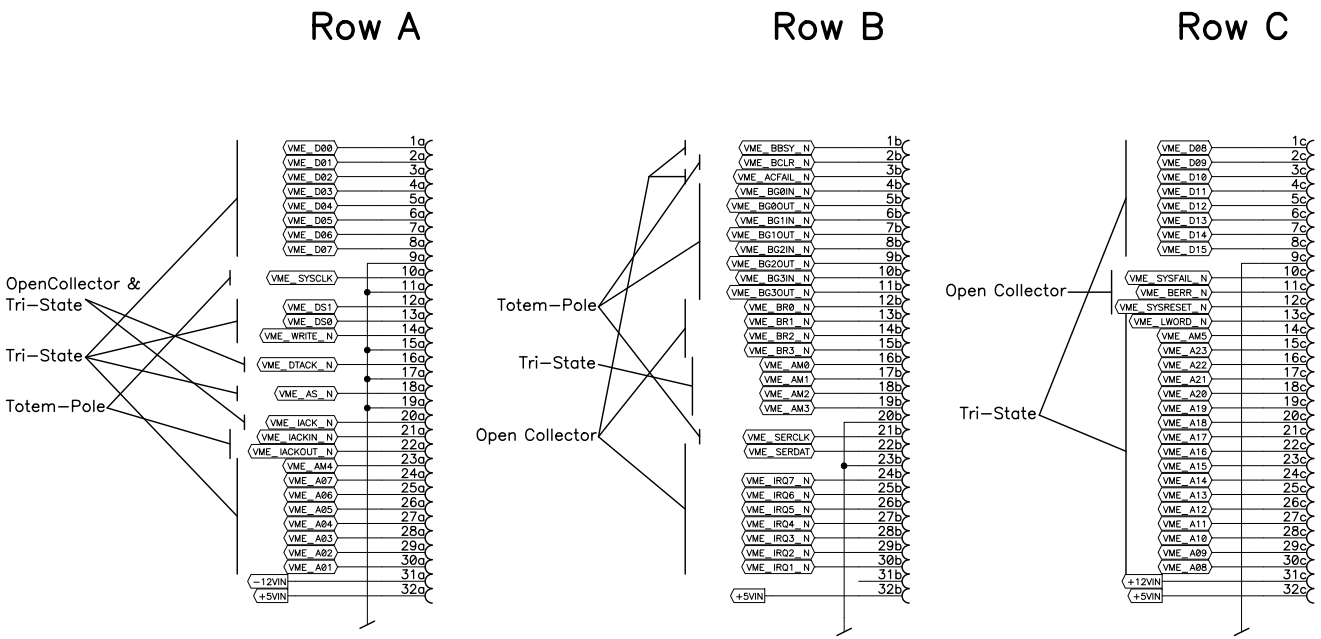


IGORIII: +1.3818V (R16 = 11k; R17 = 5.6k)
MOLIS: +4.096V (R16 = 0; R17 = 00)

ADC / DAC Board Molis & IGOR III Reference	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	5/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

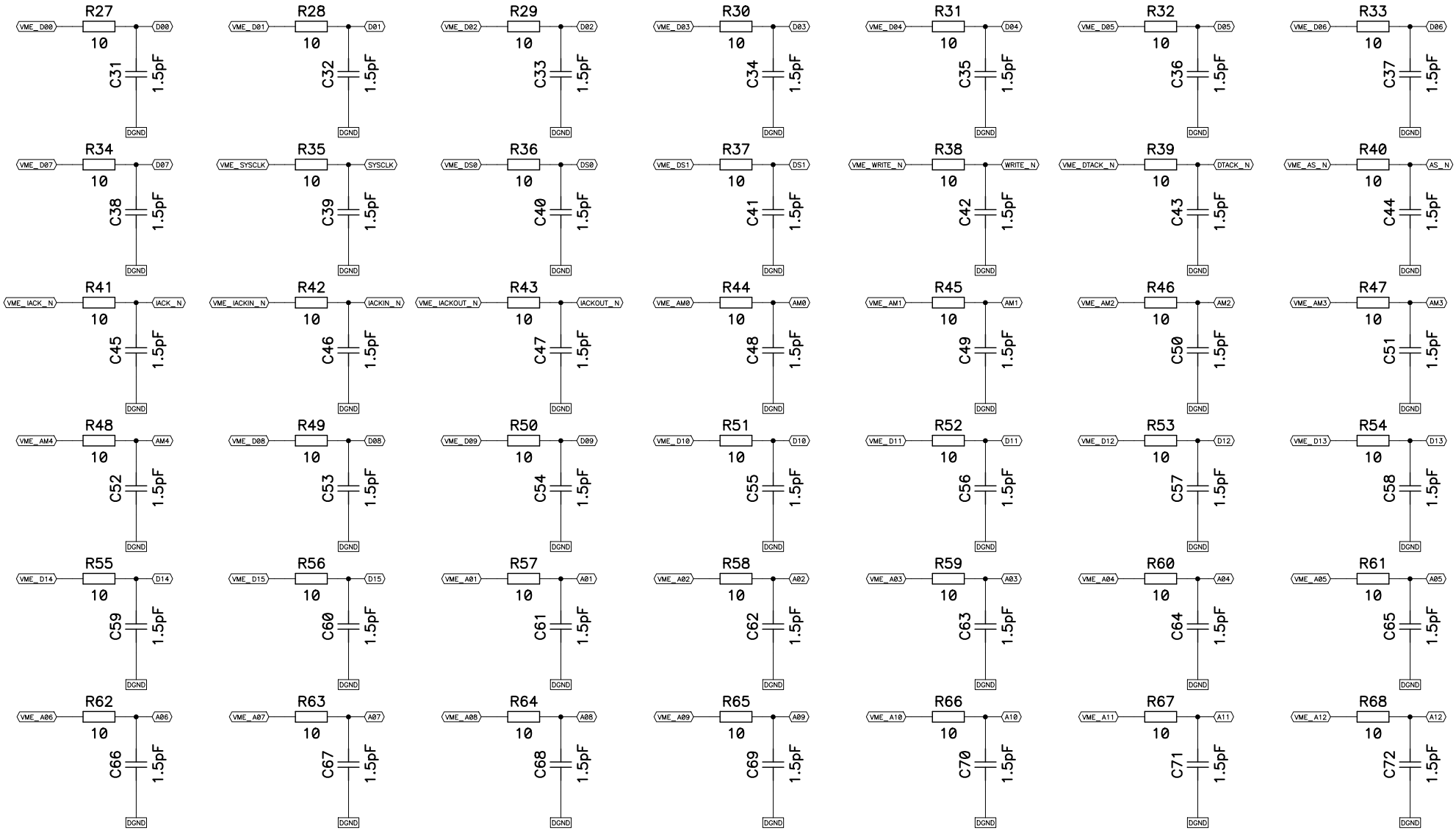
VME 96 pins

3x32 pins VME compatible backplane connector



ADC / DAC Board Molis & IGOR III VME Connector	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	6/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

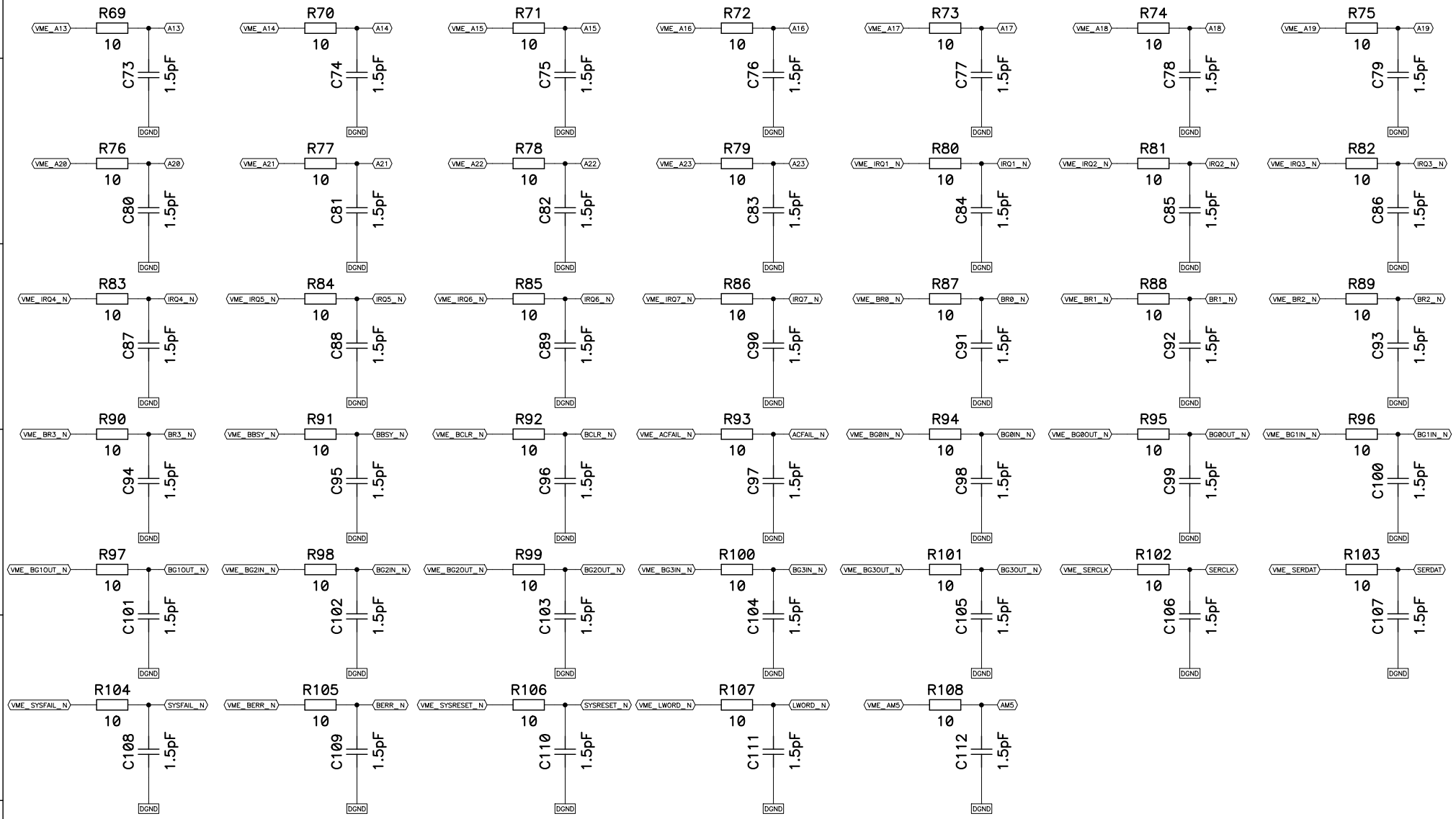
Digital Line Filters 1



- Filter high frequency parts to avoid injection of erros on the board.
- Cutoff frequency approx. 10GHz
- Filters have to be placed the nearest possible to the mezzanine connector

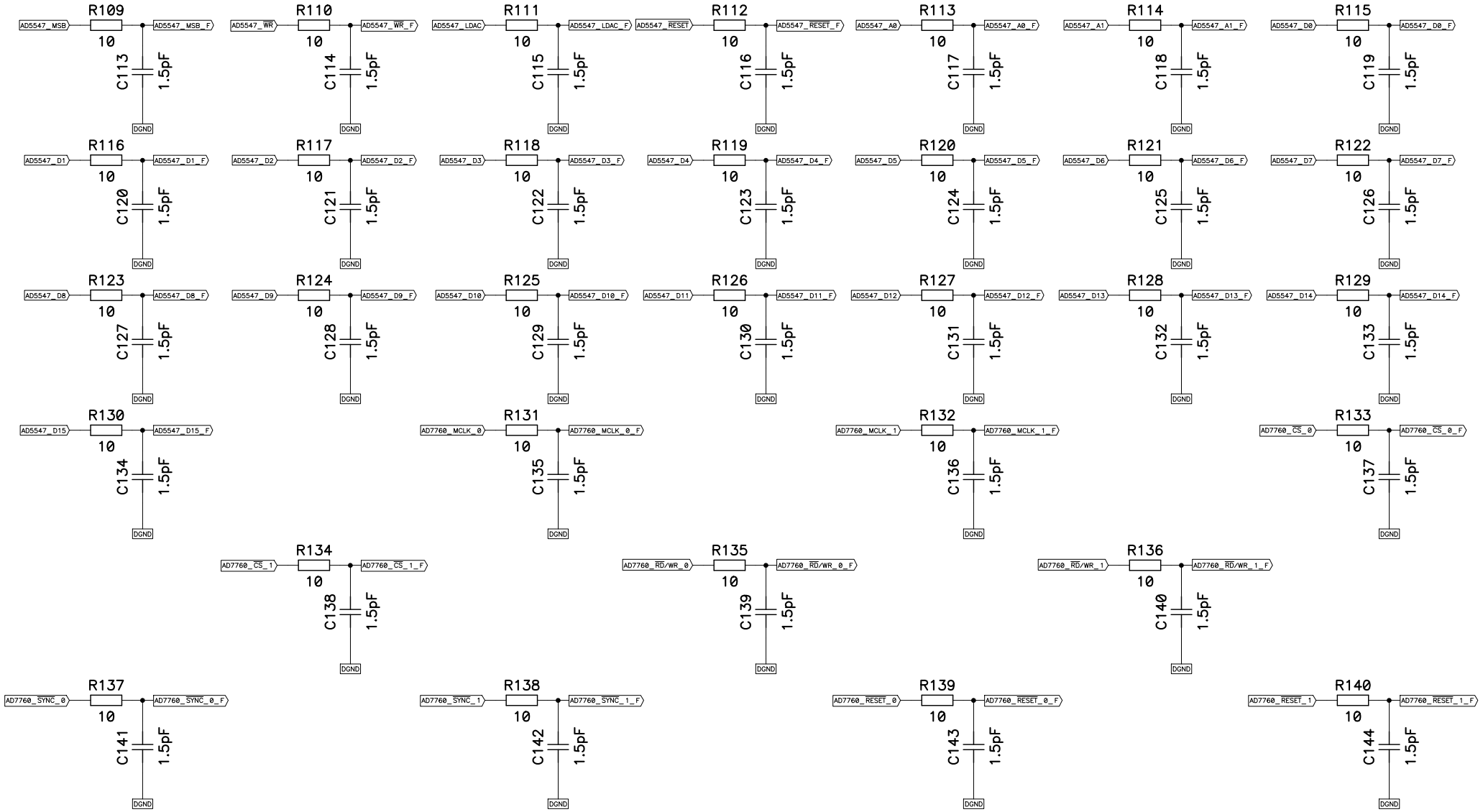
ADC / DAC Board Molis & IGOR III — Digital Line Filters 1	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	7/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

Digital Line Filters 2



ADC / DAC Board Molis & IGOR III — Digital Line Filters 2	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	8/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

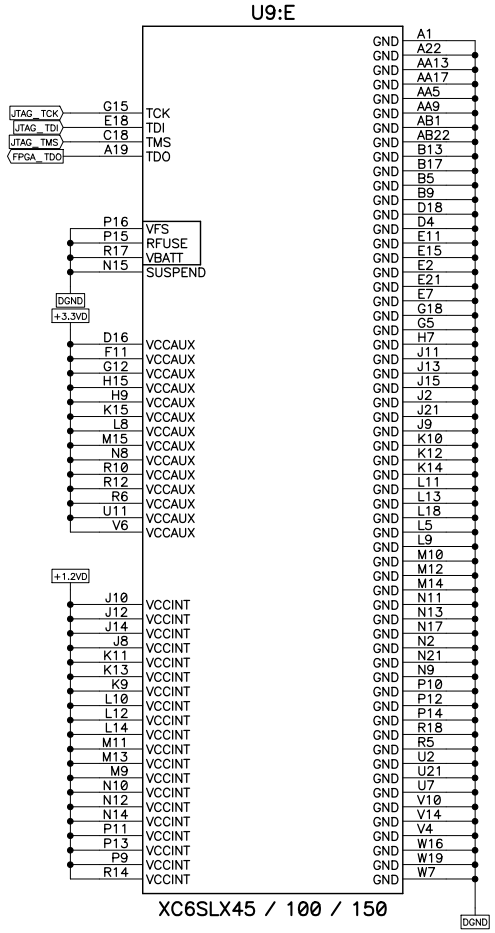
Digital Line Filters 3



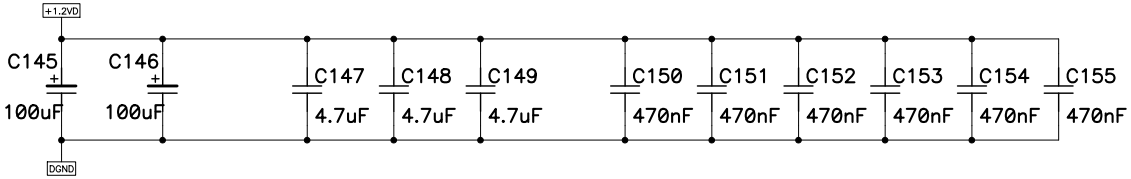
ADC / DAC Board Molis & IGOR III — Digital Line Filters 3	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	9/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

FPGA Power

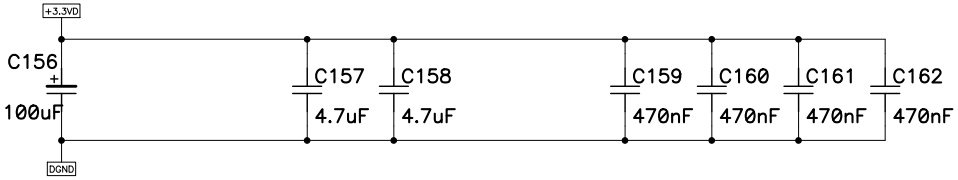
Pins NOT AVAILABLE ON LX45
ONLY AVAILABLE ON LX100 / 150
- VFS
- RFUSE
- VBATT



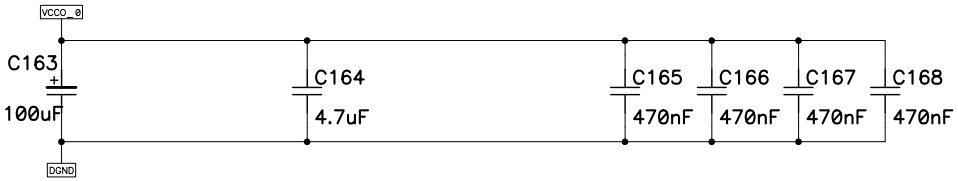
VCCINT Decoupling
LX45 –> 1x100uF / 1x4.7uF / 2x0.47uF
LX100 –> 1x100uF / 2x4.7uF / 4x0.47uF
LX150 –> 2x100uF / 3x4.7uF / 6x0.47uF



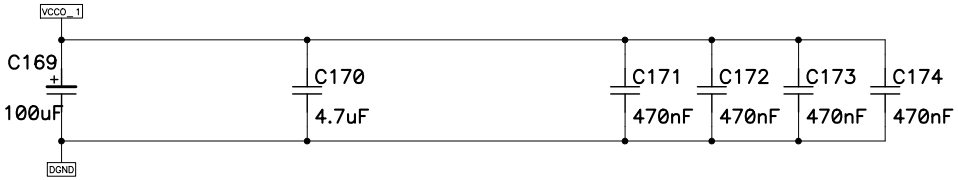
VCCAUX Decoupling
LX45, LX100, LX150 –> 1x100uF / 2x4.7uF / 4x0.47uF



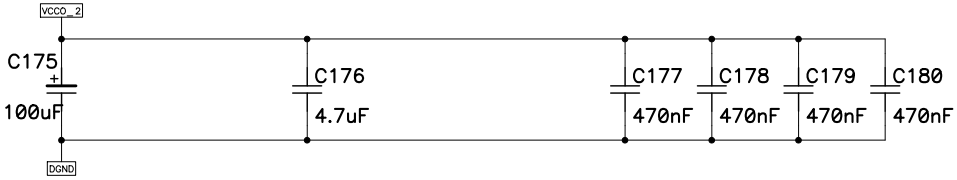
VCC0 Bank 0 Decoupling
LX45, LX100, LX150 –> 1x100uF / 1x4.7uF / 2x0.47uF



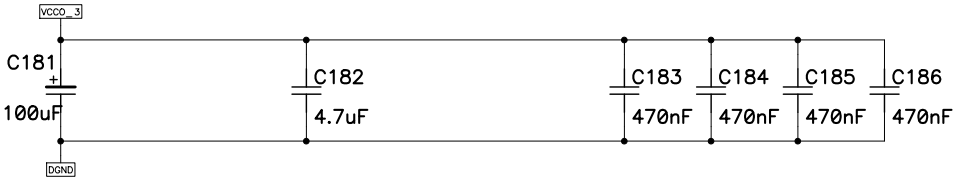
VCC0 Bank 1 Decoupling
LX45, LX100, LX150 –> 1x100uF / 1x4.7uF / 3x0.47uF



VCC0 Bank 2 Decoupling
LX45 –> 1x100uF / 1x4.7uF / 4x0.47uF
LX100, LX150 –> 1x100uF / 1x4.7uF / 3x0.47uF



VCC0 Bank 3 Decoupling
LX45, LX100, LX150 –> 1x100uF / 1x4.7uF / 3x0.47uF



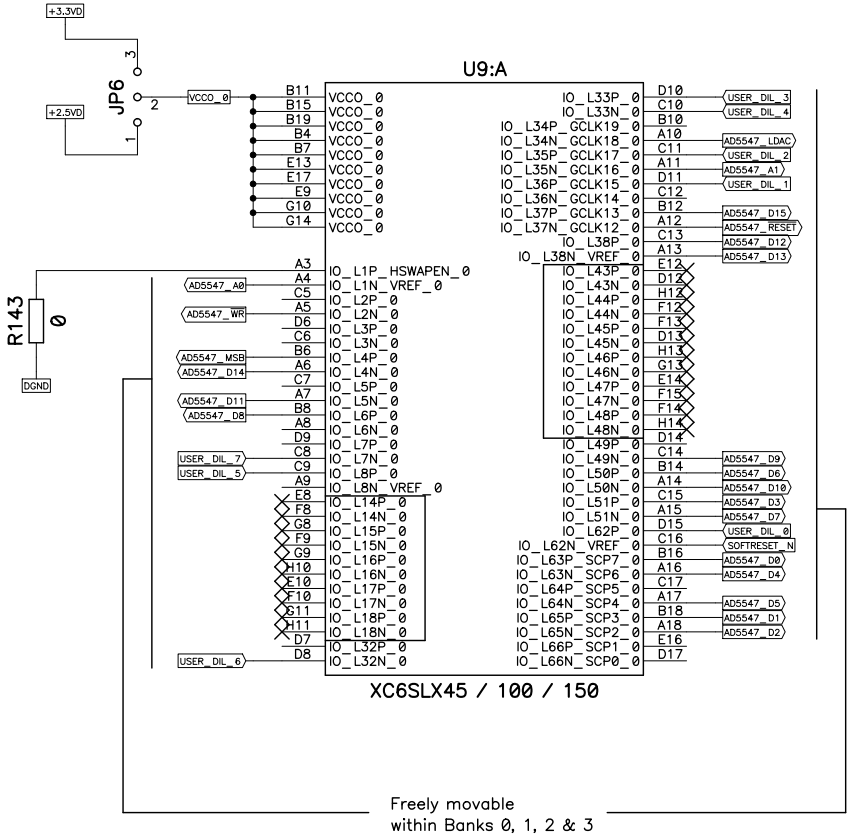
ADC / DAC Board Molis & IGOR III — FPGA Power	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	10/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

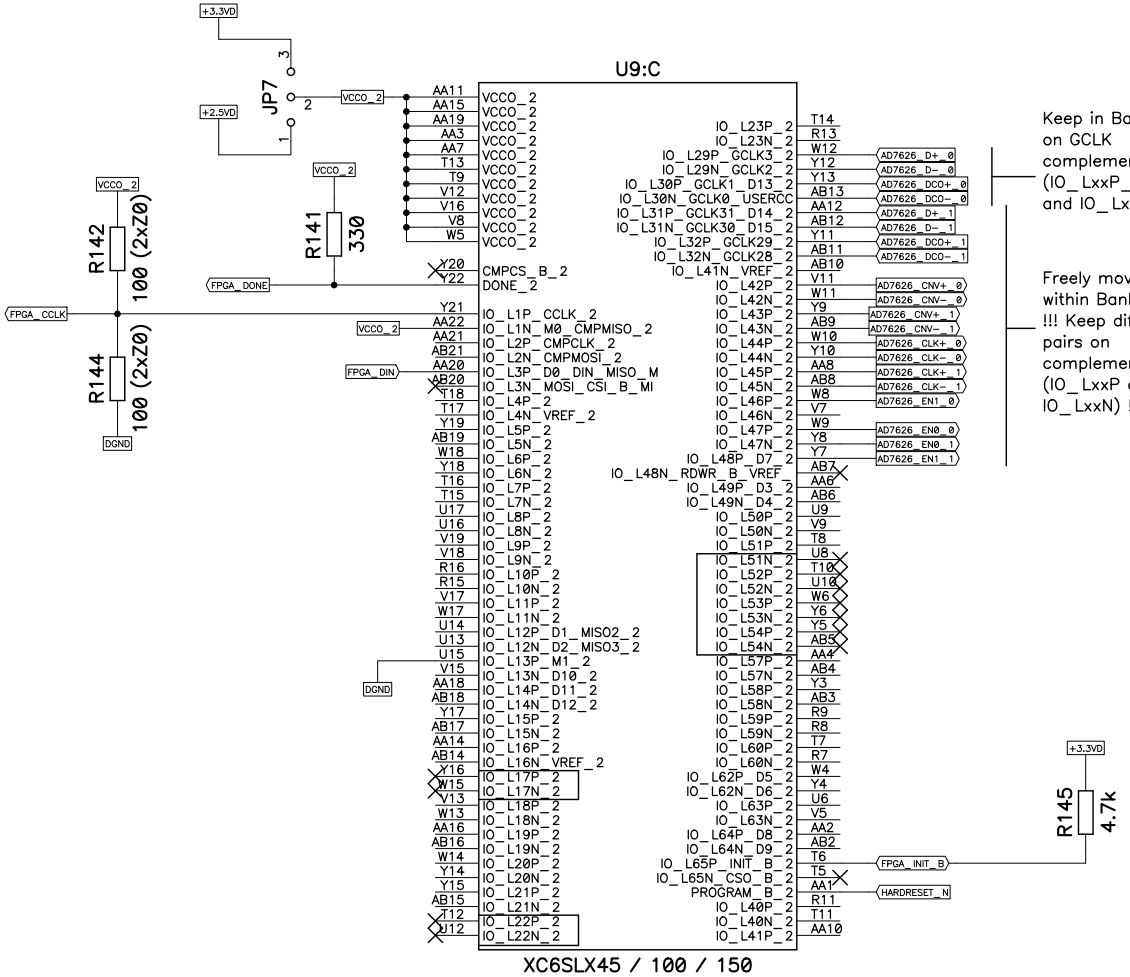
FPGA Bank 0 & 2

Pins NOT AVAILABLE ON LX45
ONLY AVAILABLE ON LX100 / 150
- IO_L14P_0, IO_L14N_0, IO_L15P_0, IO_L15N_0, IO_L16P_0, IO_L16N_0, IO_L17P_0, IO_L17N_0, IO_L18P_0

BPI Programming mode
M0 = 0
M1 = 0

Pins NOT AVAILABLE ON LX100
ONLY AVAILABLE ON LX45 / 150
- IO_L17P_2, IO_L17N_2
- IO_L22P_2, IO_L22N_2
- IO_L51P_2, IO_L51N_2, IO_L52P_2, IO_L52N_2, IO_L53P_2, IO_L53N_2, IO_L54P_2, IO_L54N_2



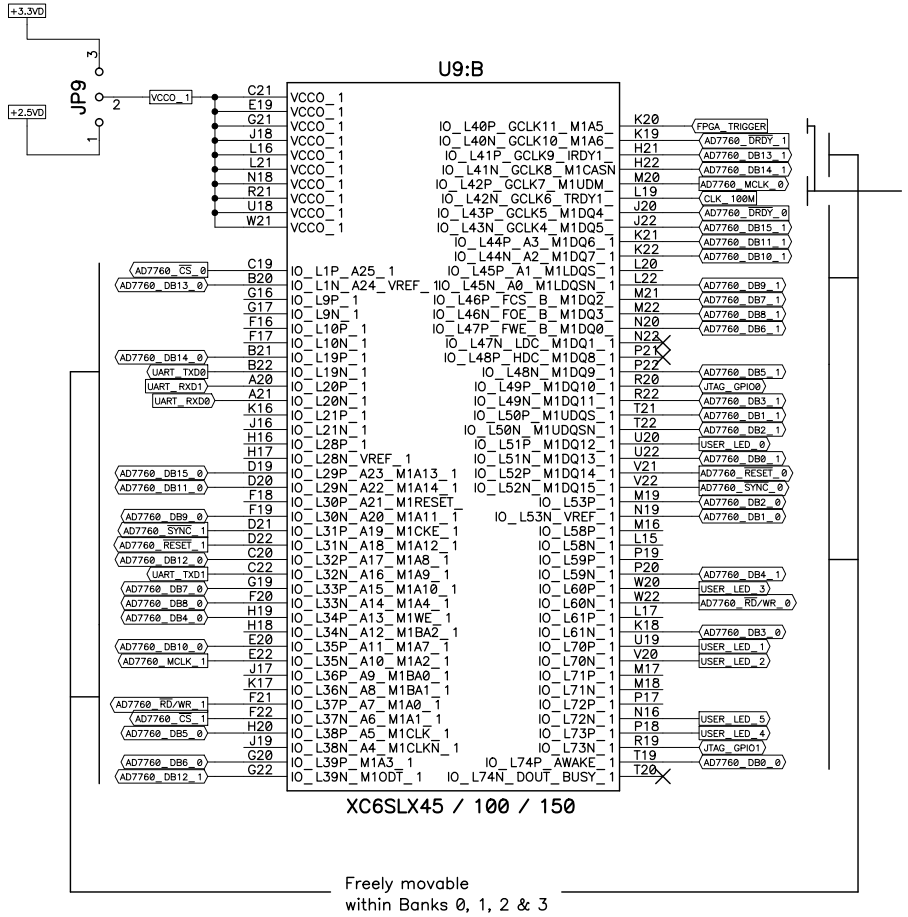


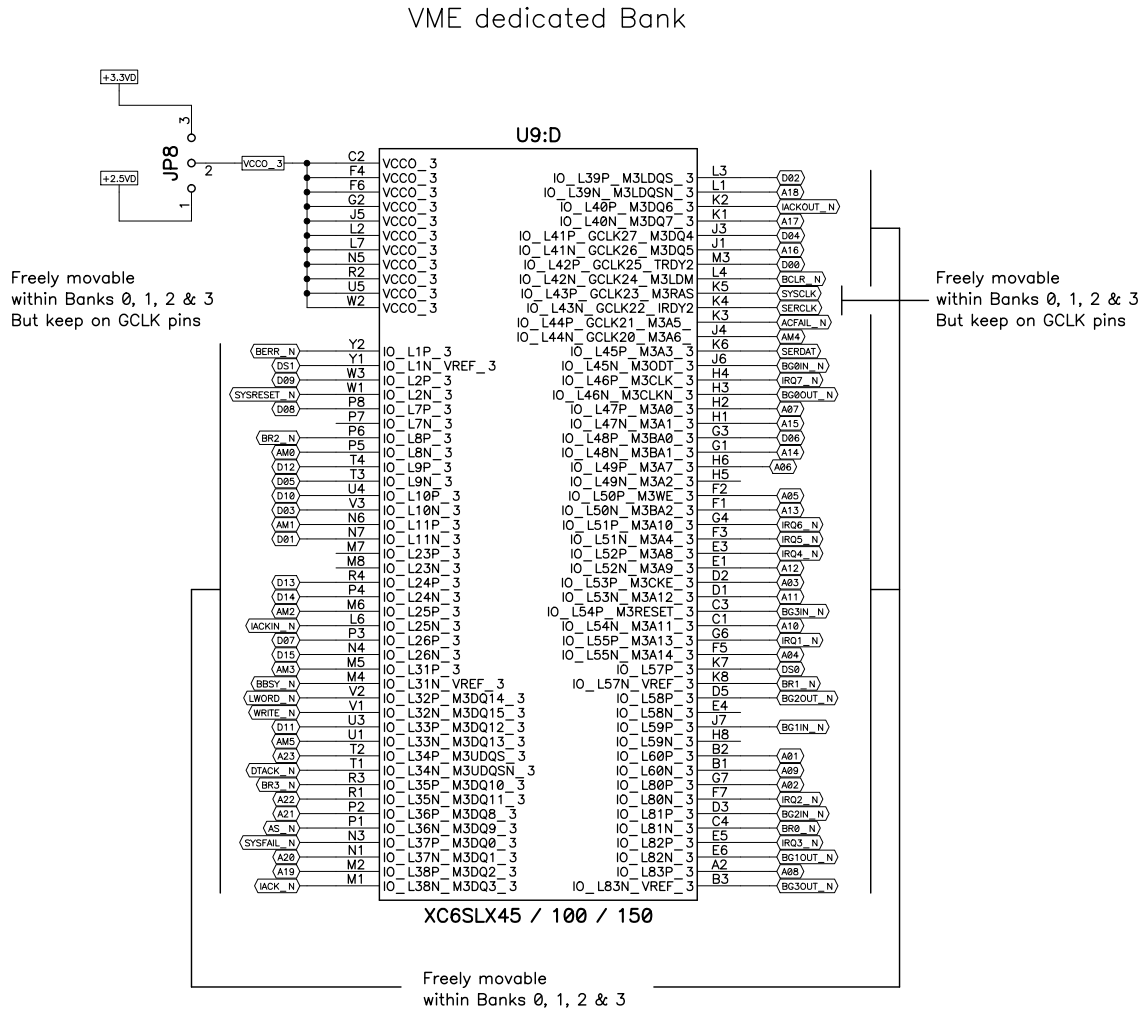
Keep in Bank 0 or 2 on GCLK complementary pins (IO_LxxP_GCLKx and IO_LxxN_GCLKx)

Freely movable within Bank 0 or 2 !!! Keep differential pairs on complementary pins (IO_LxxP and IO_LxxN) !!!

ADC / DAC Board Molis & IGOR III	FPGA 1	DES	22.10.2012 Chappot L.
		REV	V2.0
HAUTE ECOLE VALAISANNE		11/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

FPGA Bank 1 & 3

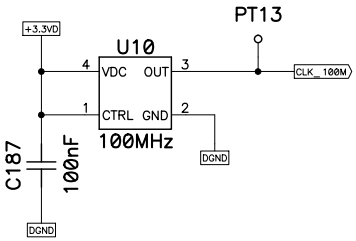




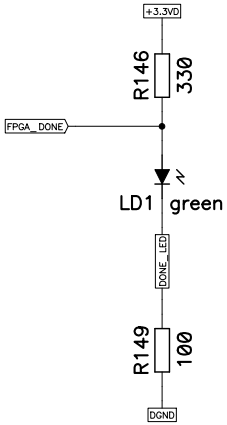
ADC / DAC Board Molis & IGOR III	FPGA 2	DES	22.10.2012 Chappot L.
		REV	V2.0
HAUTE ECOLE VALAISANNE		12/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

FPGA Config

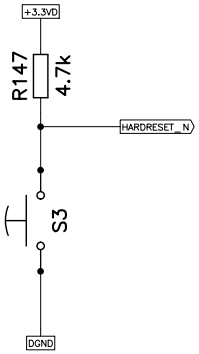
Main Oscillator



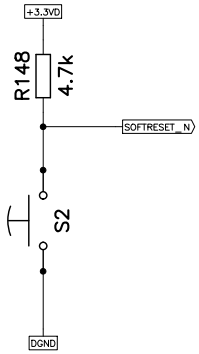
FPGA Done LED



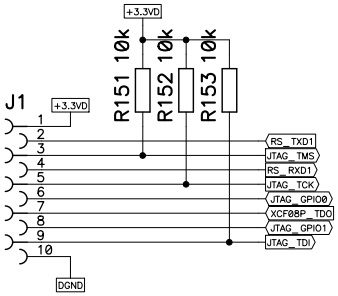
FPGA Hardreset Reprogram



FPGA Softreset

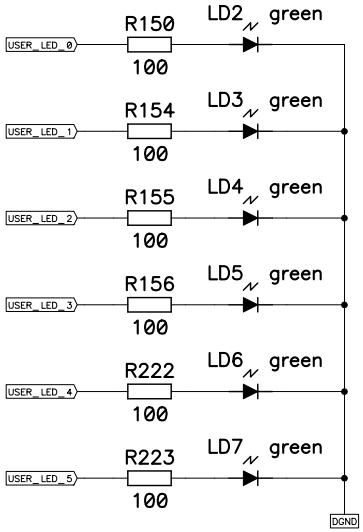


JTAG connector

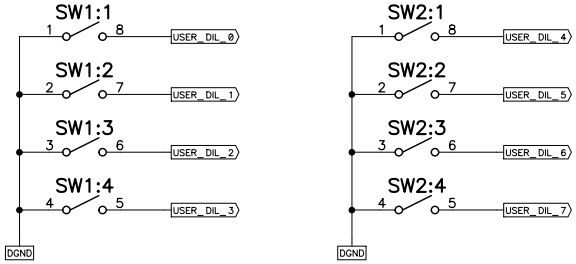


User LEDs

R = (3.3V – 2V) / 20mA = 65

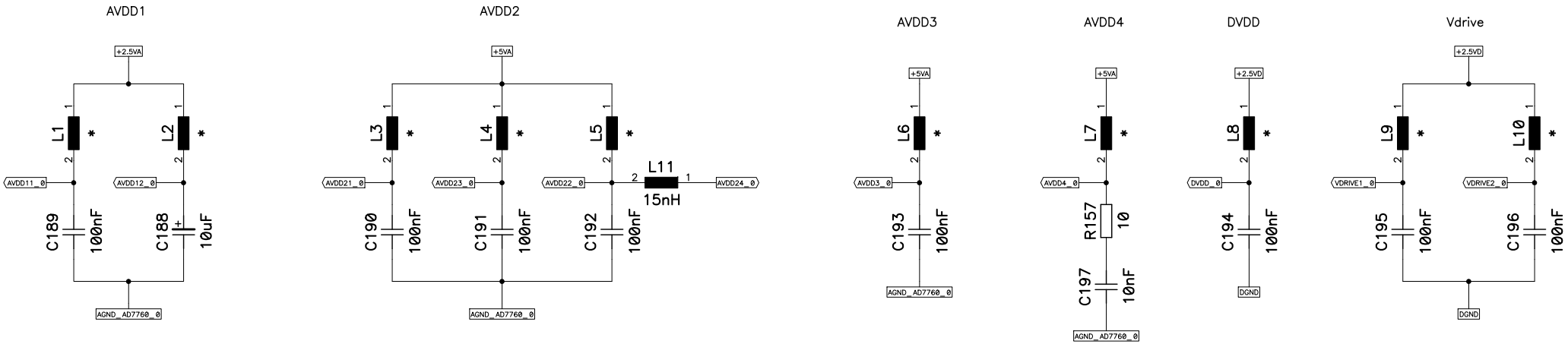


User DIP switches

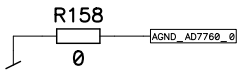


ADC / DAC Board Molis & IGOR III FPGA Config	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	13/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

ADC Channel 0: AD7760 Supply



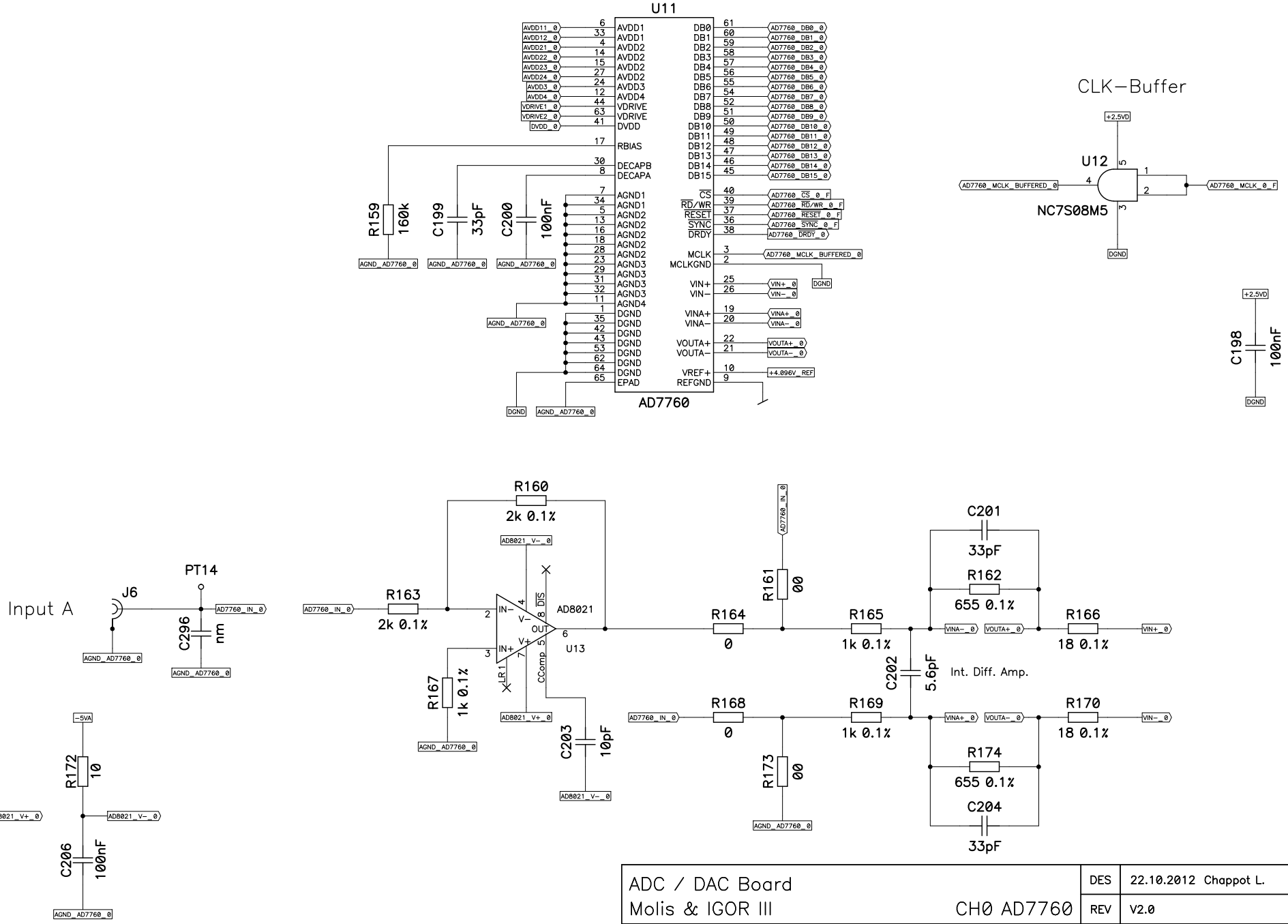
Ground bridge



*: Wuerth 74279266
(ferrit bead)

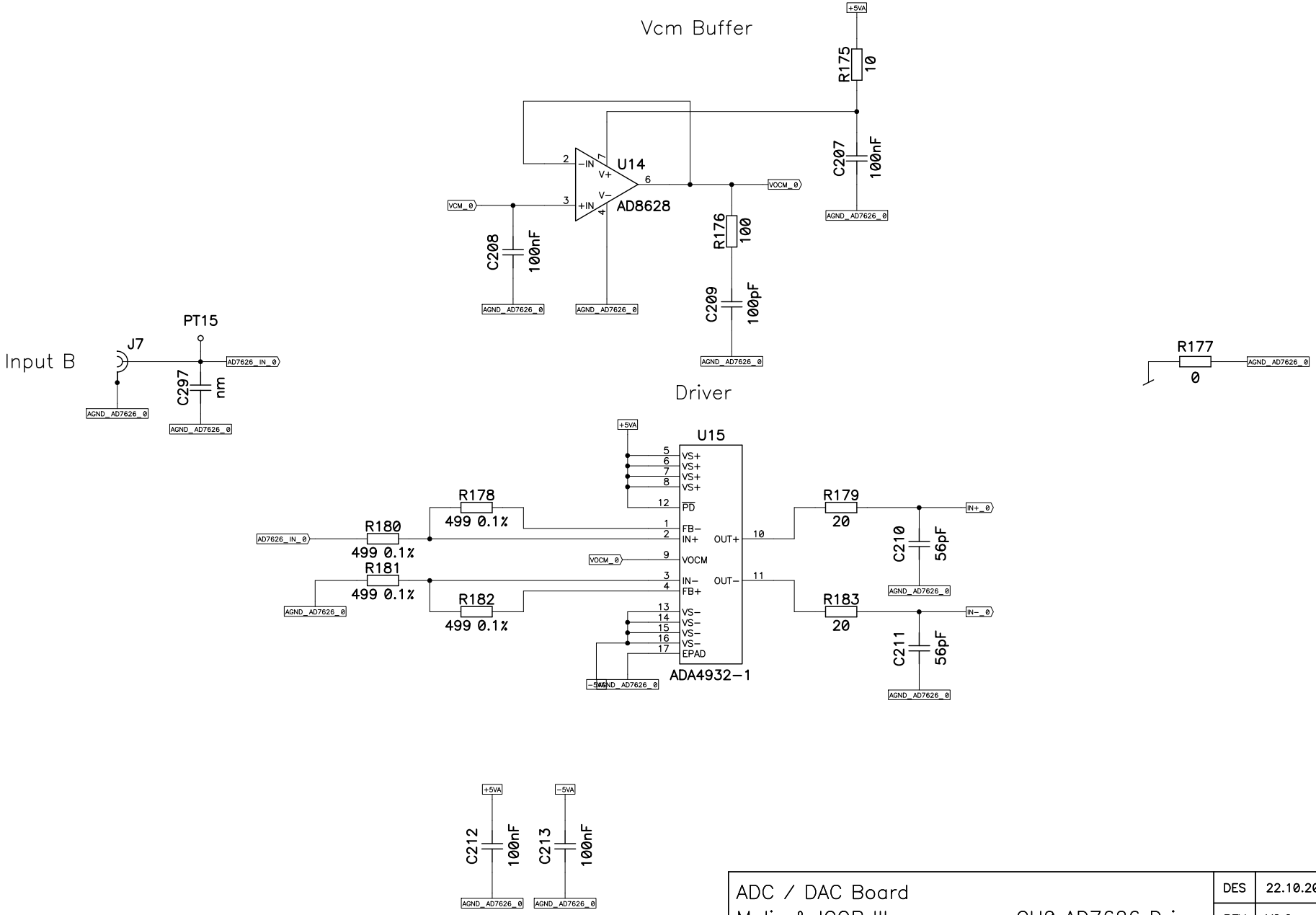
ADC / DAC Board Molis & IGOR III CH0 AD7760 Supply	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	14/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

ADC Channel 0: AD7760



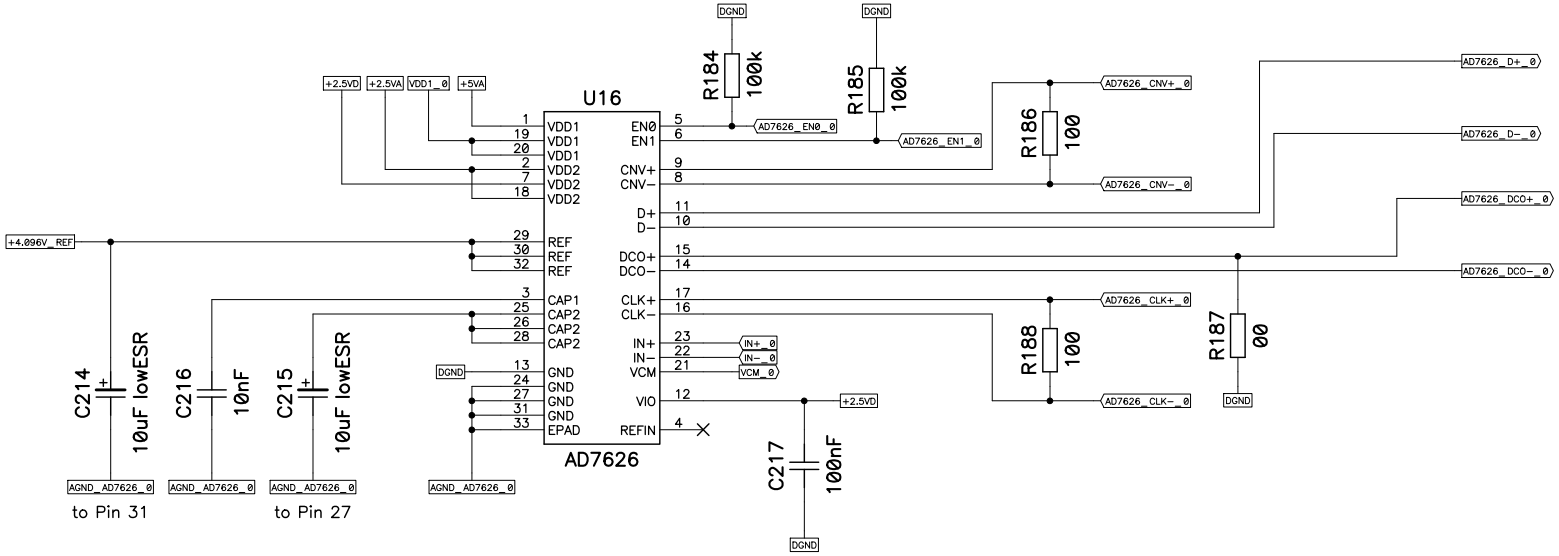
ADC / DAC Board Molis & IGOR III	CH0 AD7760	DES	22.10.2012 Chappot L.
		REV	V2.0
HAUTE ECOLE VALAISANNE		15/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

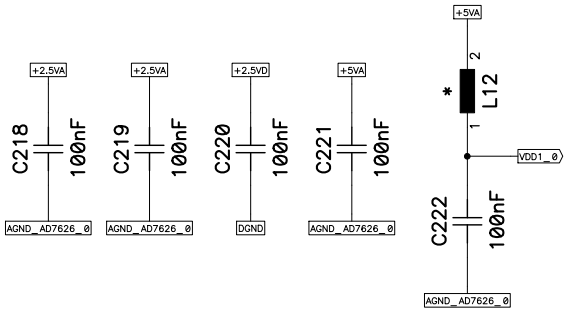
ADC Channel 0: AD7626 Driver



ADC / DAC Board Molis & IGOR III CH0 AD7626 Driver	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	16/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

ADC Channel 0: AD7626

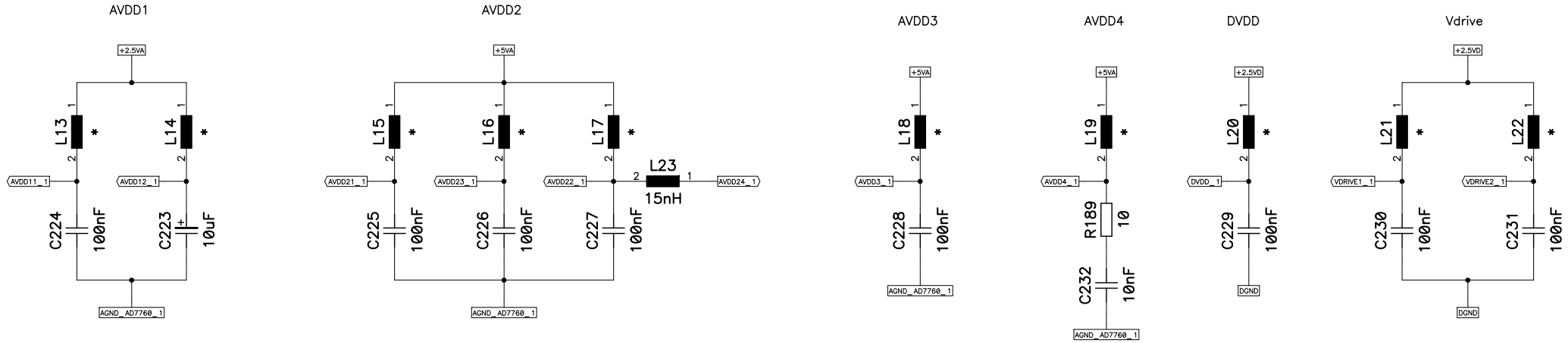




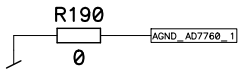
*: Wuerth 74279266
(ferrit bead)

ADC / DAC Board Molis & IGOR III CH0 AD7626	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	17/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

ADC Channel 1: AD7760 Supply

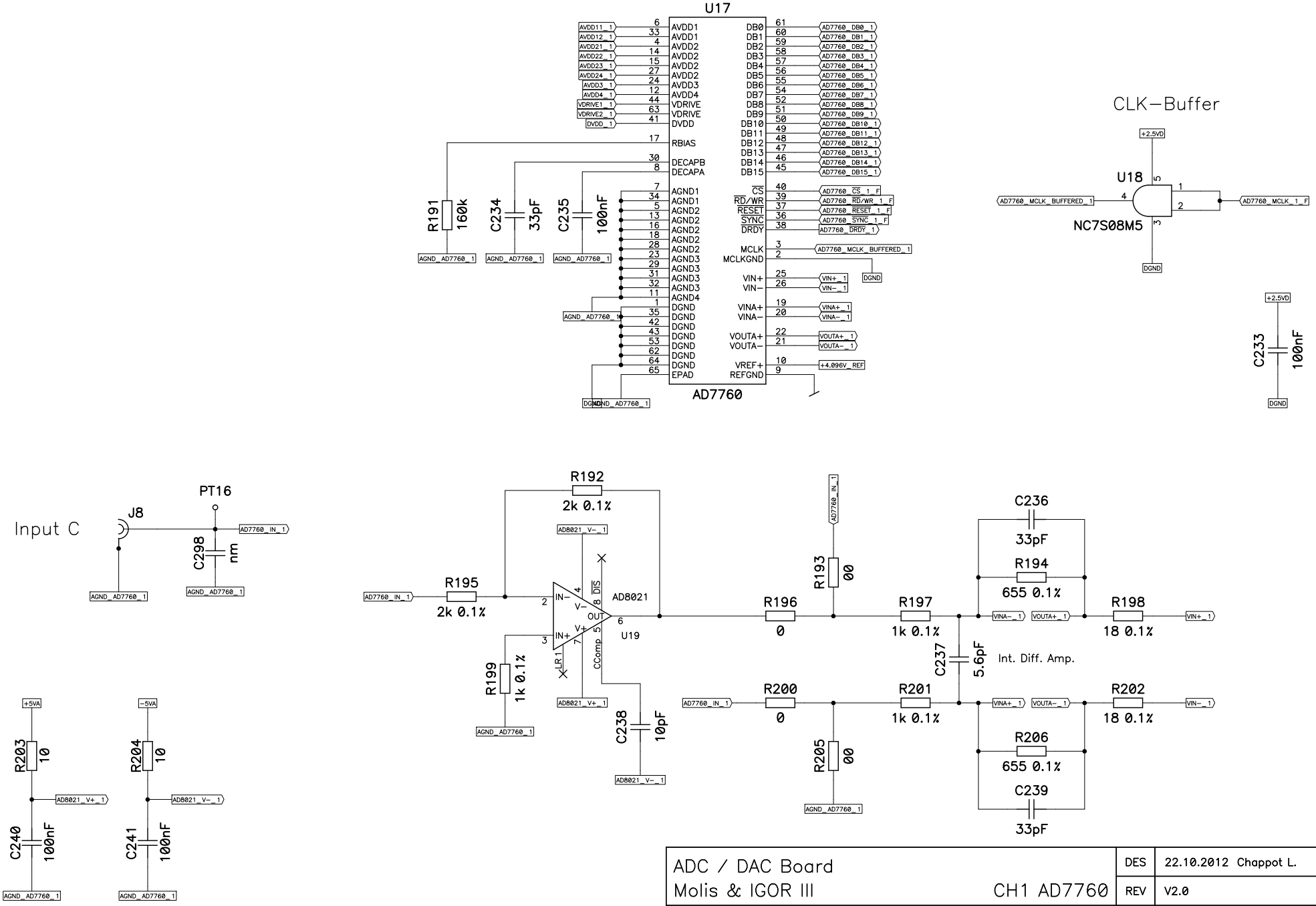


*: Wuerth 74279266
(ferrit bead)



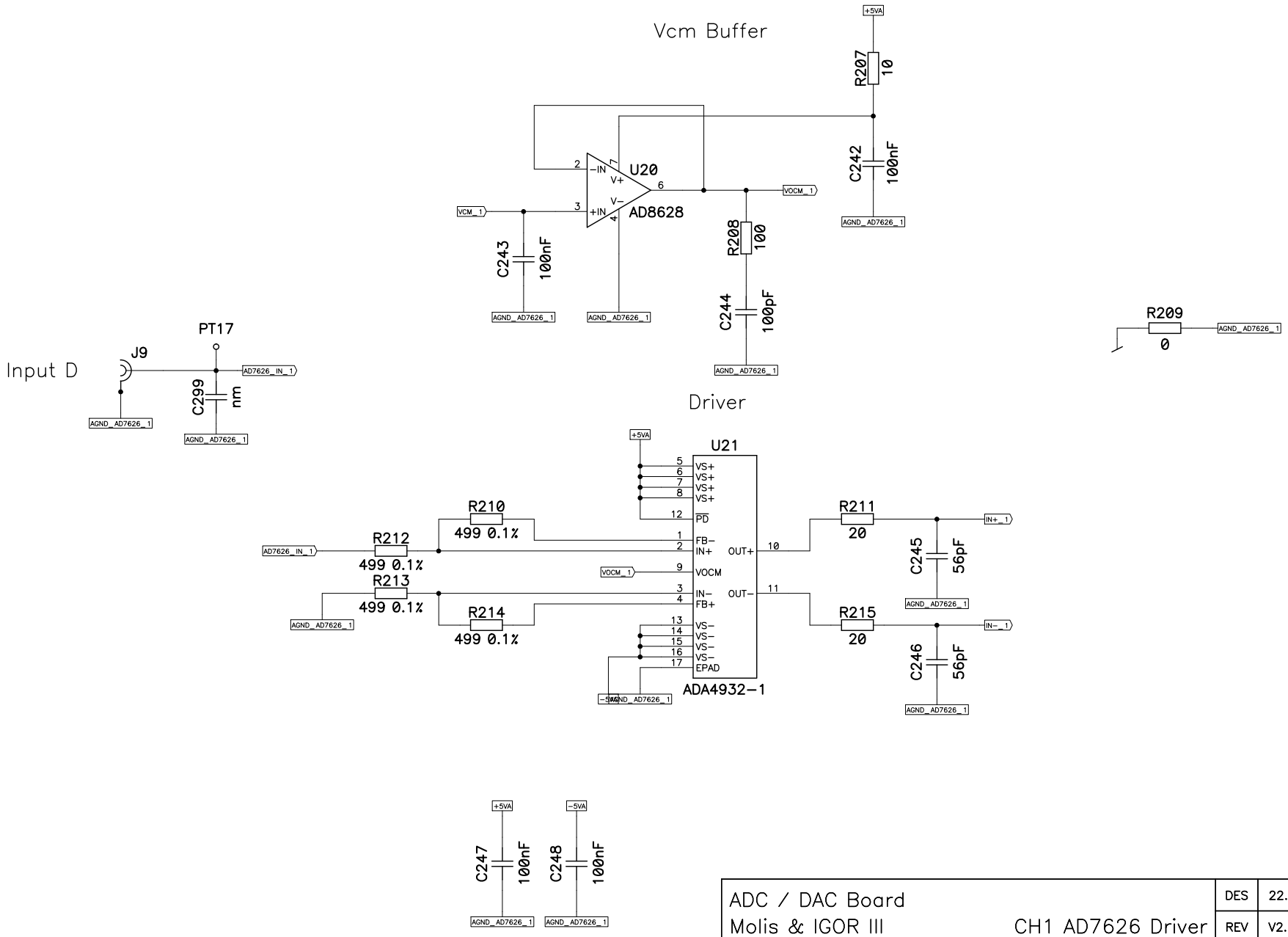
ADC / DAC Board Molis & IGOR III CH1 AD7760 Supply	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	18/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

ADC Channel 1: AD7760



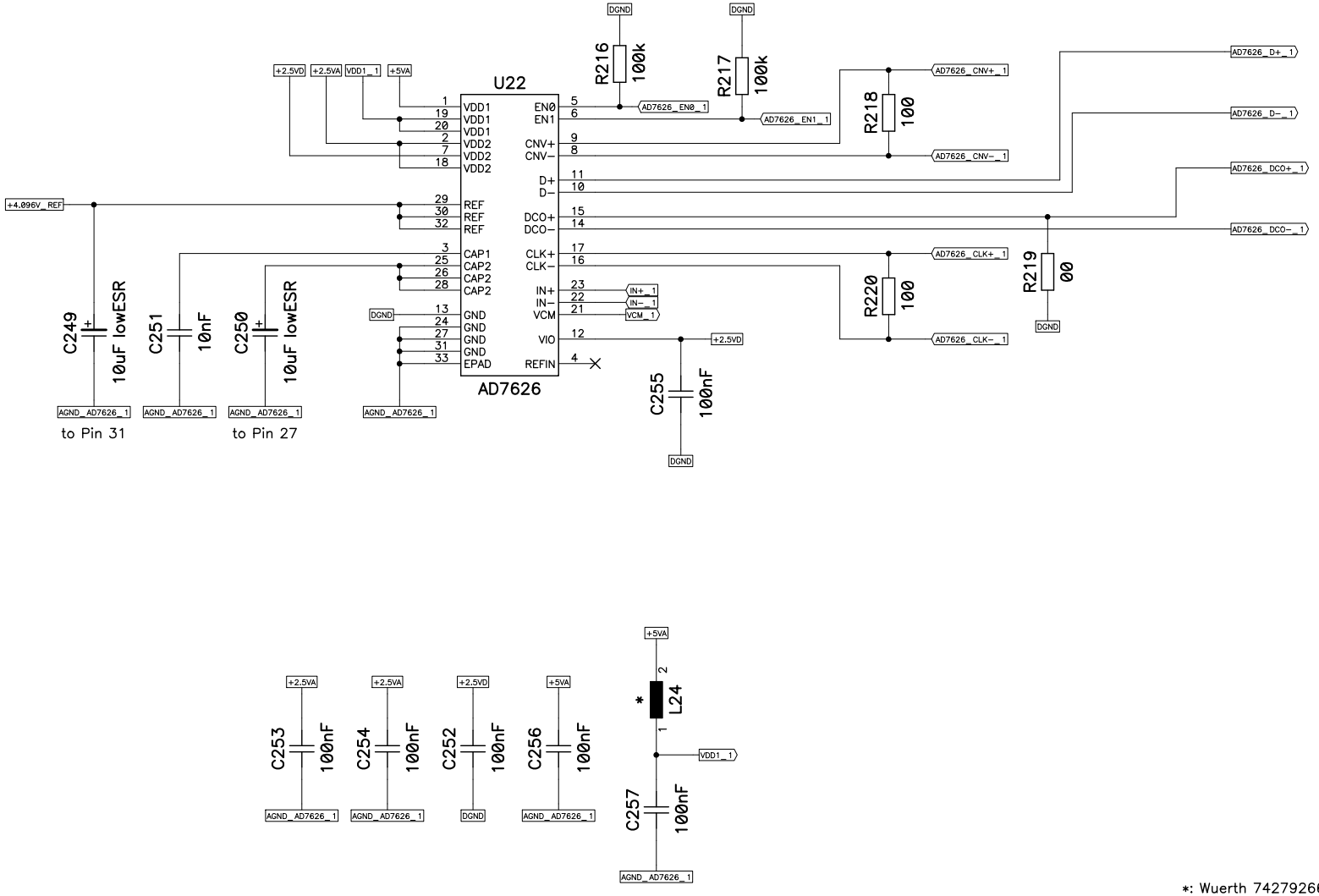
ADC / DAC Board Molis & IGOR III CH1 AD7760	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	19/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

ADC Channel 1: AD7626 Driver



ADC / DAC Board Molis & IGOR III CH1 AD7626 Driver	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	20/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

ADC Channel 1: AD7626

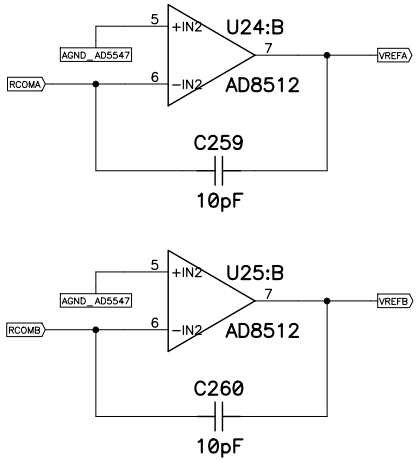


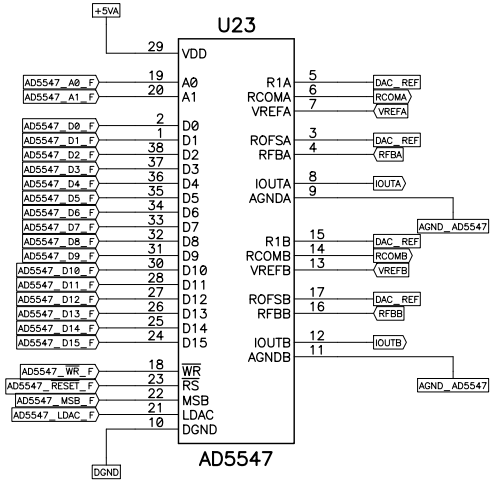
*: Wuerth 74279266
(ferrit bead)

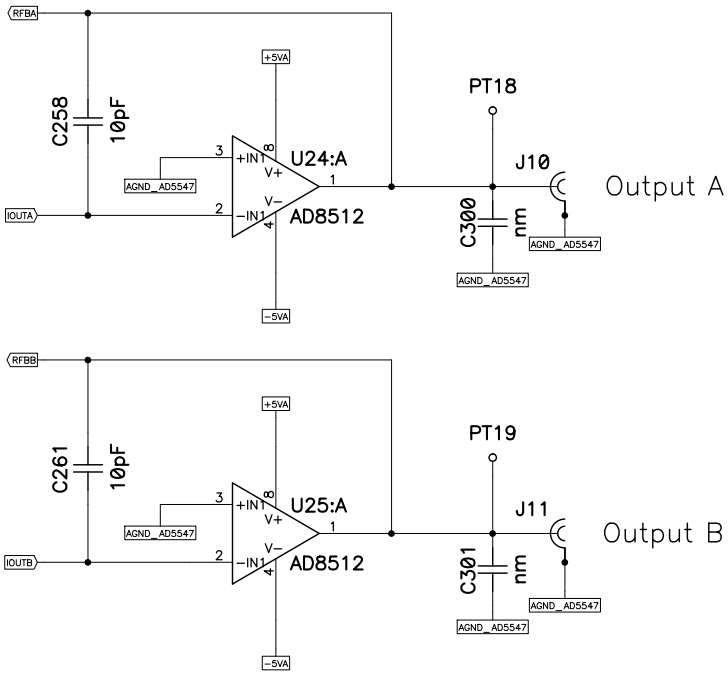
ADC / DAC Board Molis & IGOR III	CH1 AD7626	DES	22.10.2012 Chappot L.
		REV	V2.0
HAUTE ECOLE VALAISANNE		21/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

DAC AD5547

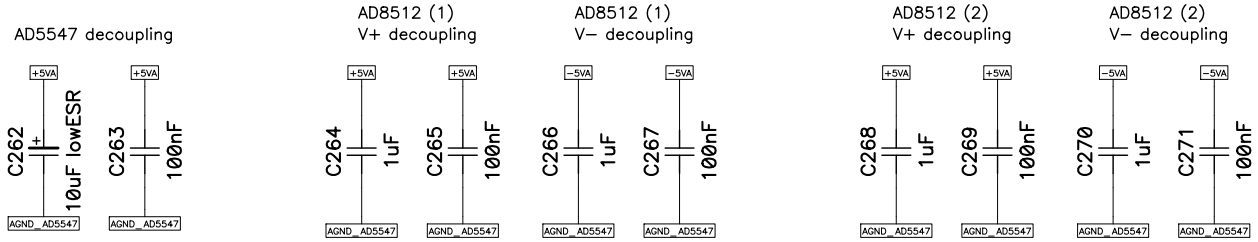
DAC

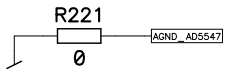






Decoupling



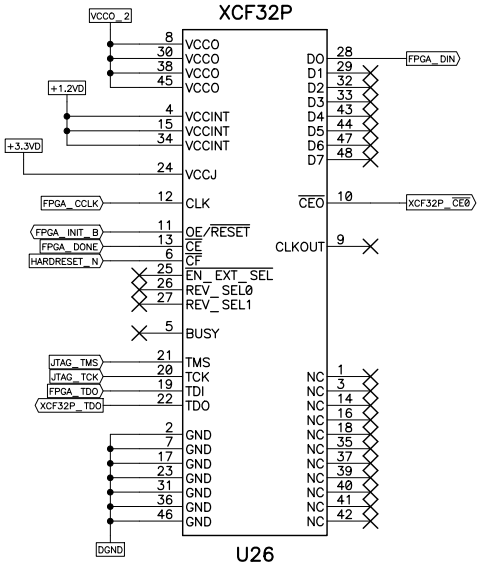


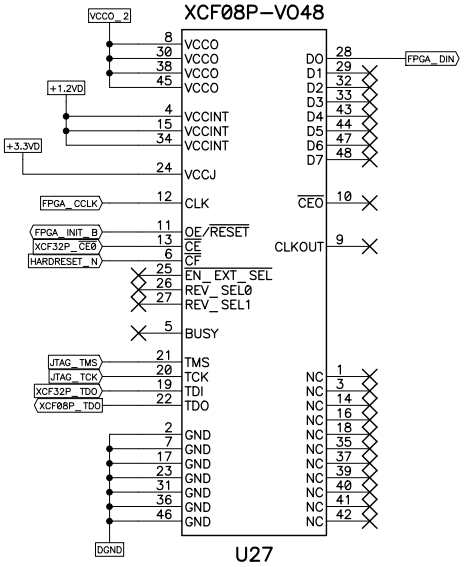
Bipolar Output (4−Quadrant Multiplying Mode)
IGORIII Output: 0.975Vrms (1kHz − 200kHz)
IGORIII Reference: +1.3795V

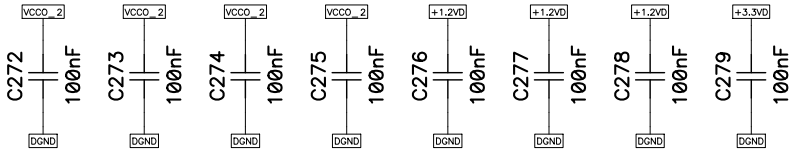
ADC / DAC Board Molis & IGOR III AD5547	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	22/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

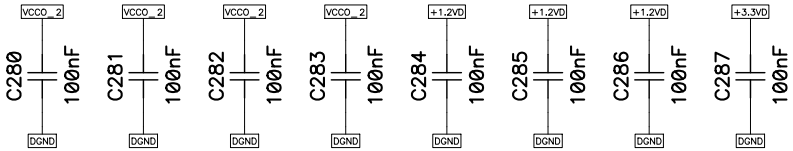
Flash Memory

FPGA in Master Serial mode
with 2 cascaded XCFxxP PROMs





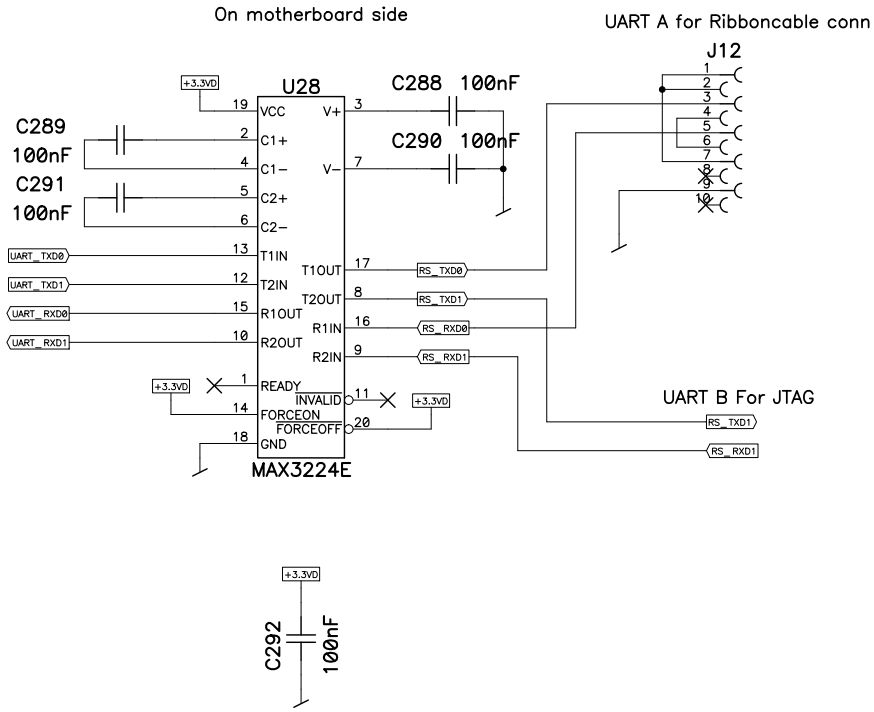




ADC / DAC Board Molis & IGOR III — Memory	DES	22.10.2012 Chappot L.
	REV	V2.0
HAUTE ECOLE VALAISANNE	23/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch

RS-232

RS 232 Serial ports



ADC / DAC Board Molis & IGOR III	RS-232	DES	22.10.2012 Chappot L.
		REV	V2.0
HAUTE ECOLE VALAISANNE		24/24	P:\PCB\Student\TSTD\Chappot_Ludovic AD_DA_V2_0_GAS.sch