A2F-DEV-KIT

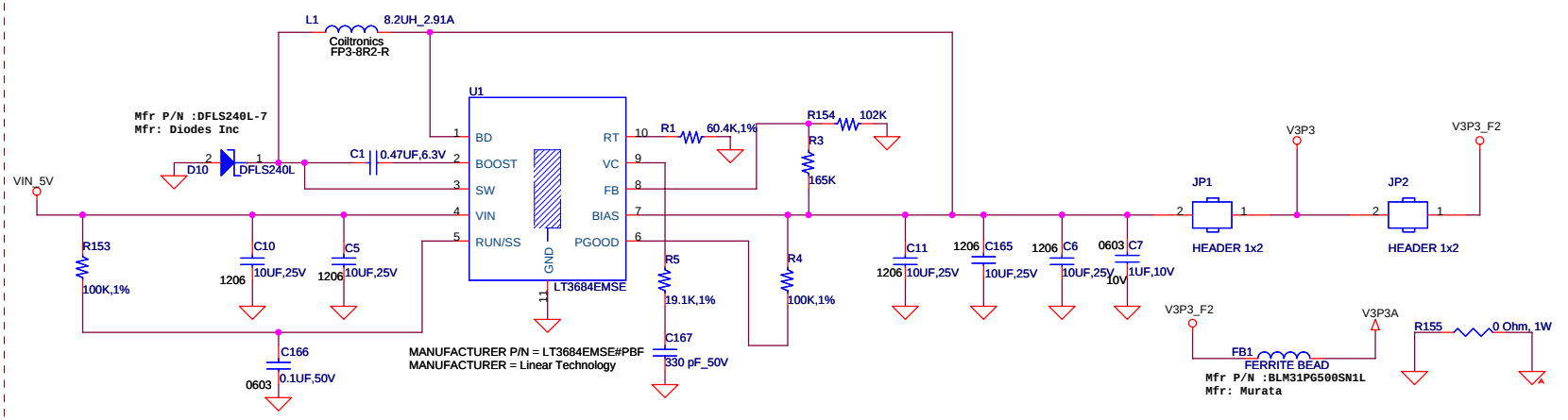
DVP-100-000-288-001 REV F

lead-free

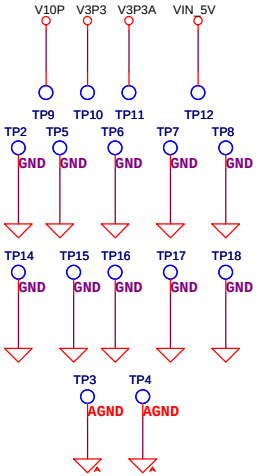
Project Name: A2F-DEV-KIT		
Rev: F	Part Number: ACTEL:DVP-100-000-288-001	PACTRON: 305-PD-10-237
Originator: LINGAMOORTHI ARUMUGAM		
Size: B	Date: Tuesday, March 30, 2010	Sheet 1 of 35

POWER SUPPLY REGULATORS 3.3V & 5V

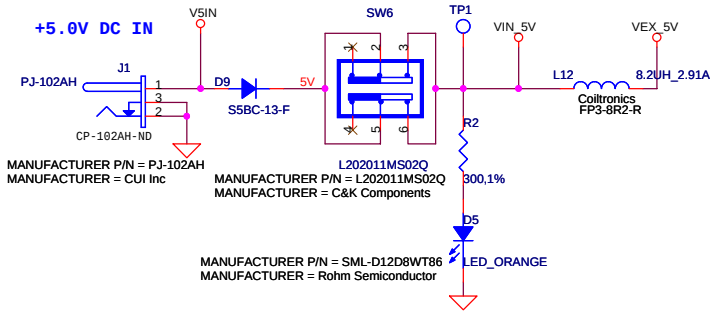
5V TO 3.3V LOGIC @ 2A



PWR & GND TEST POINTS



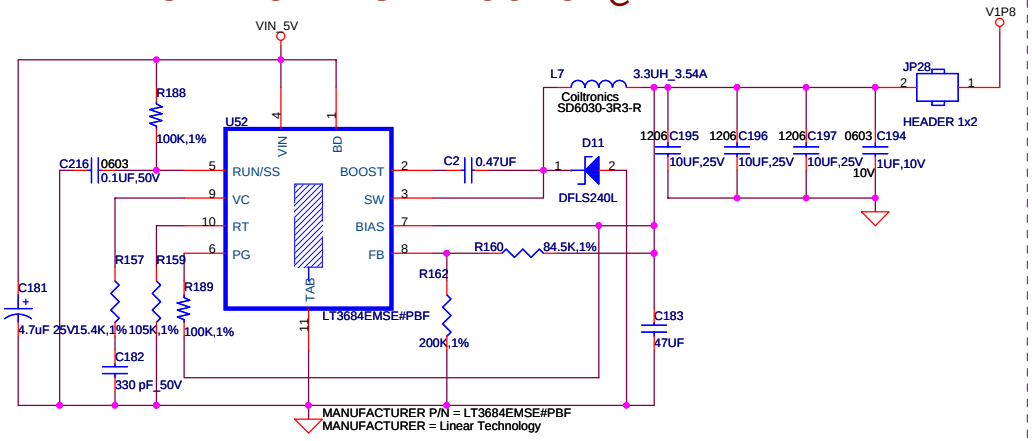
5V JACK SUPPLY



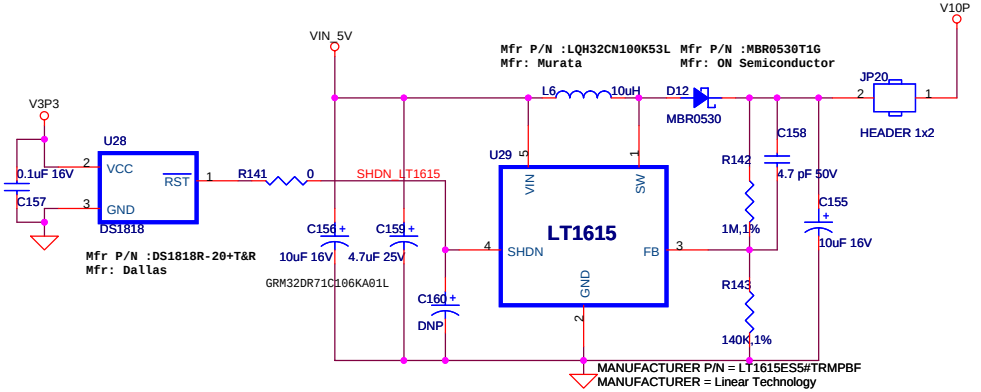
Actel		
Title: A2F-DEV-KIT		
Size: B	Document Number: POWER SUPPLY REGULATORS 3.3V & 5V	Rev: F
Date: Tuesday, March 30, 2010	Sheet 2 of 35	

Power 1.8V,10V,15V & 1.5V

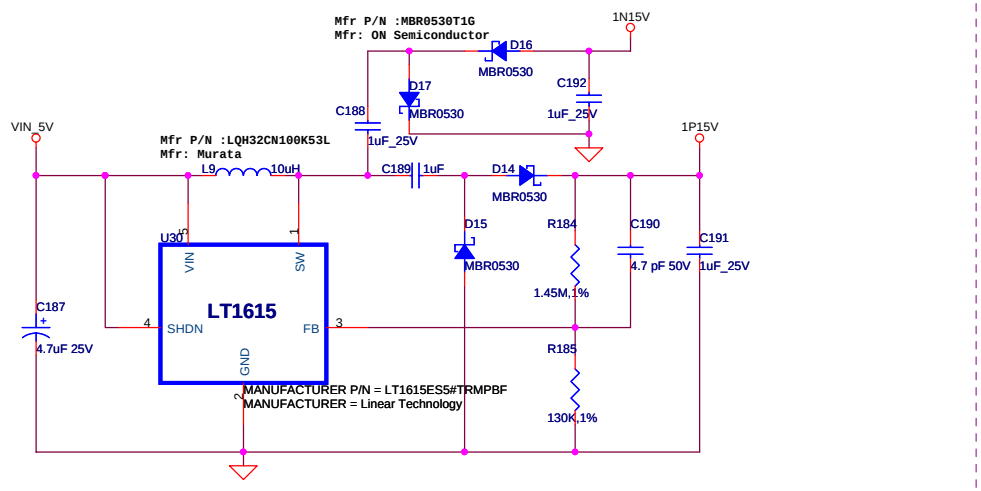
5V TO 1.8V LOGIC @ 2A



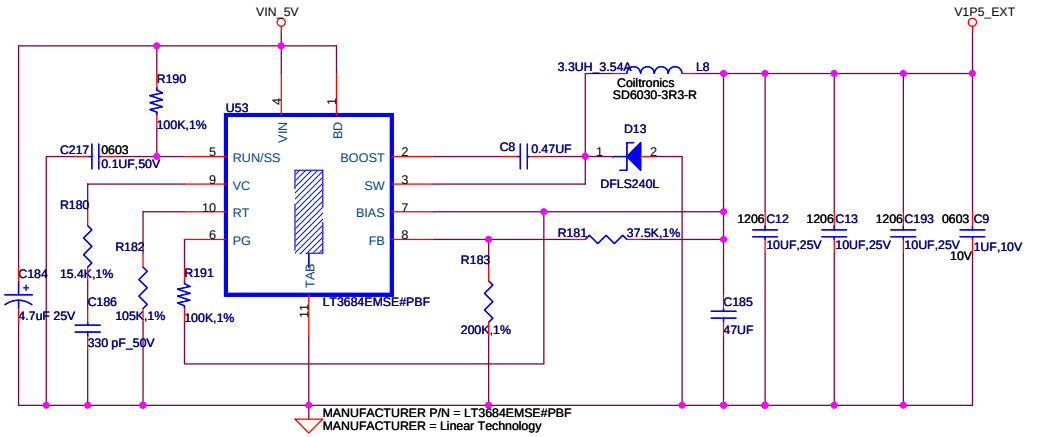
5V TO 10V @ 100mA OLED



5V TO +/-15V LOGIC @ 4mA



5V TO 1.5V LOGIC @ 2A



Actel

Title	A2F-DEV-KIT	
Size B	Document Number Power 1.8V,10V,15V & 1.5V	Rev F
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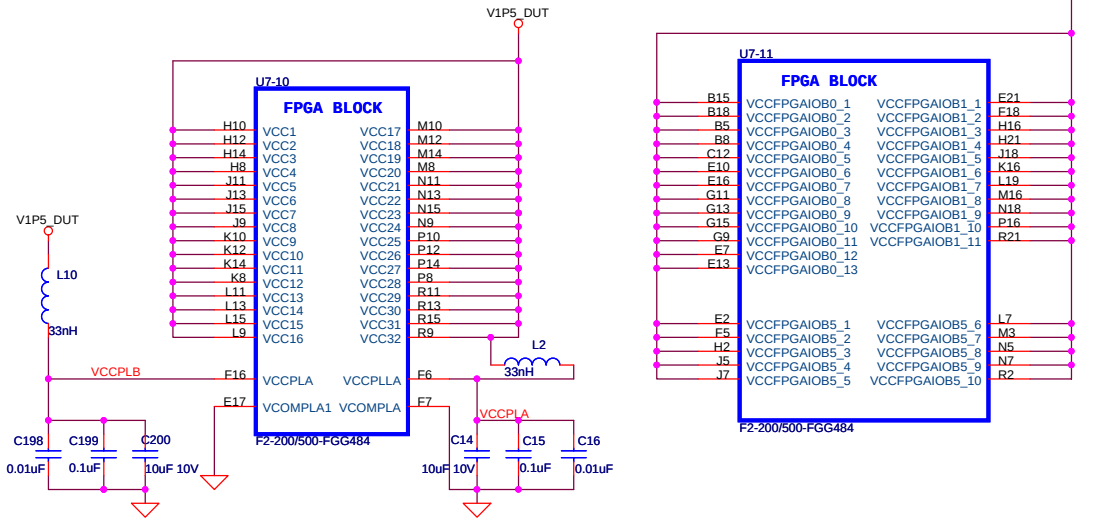
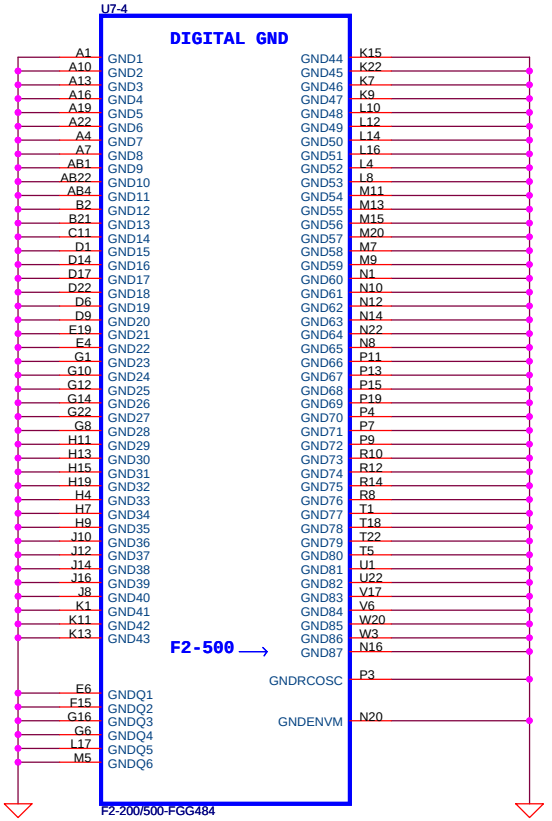
DIGITAL PWR & GND

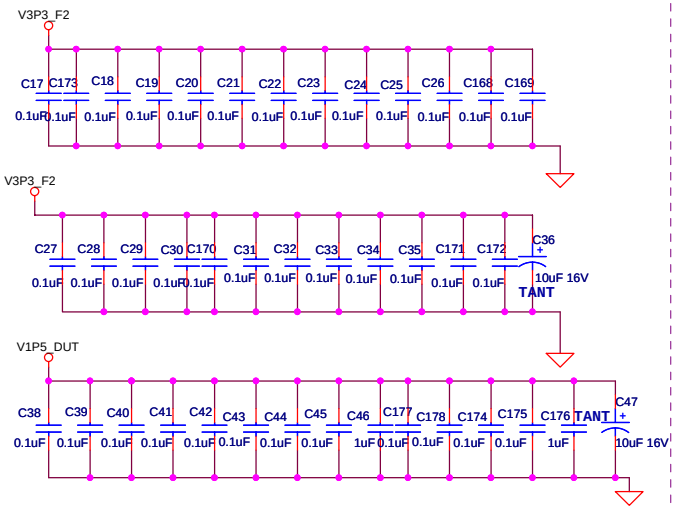
FPGA BLOCK POWER SUPPLY



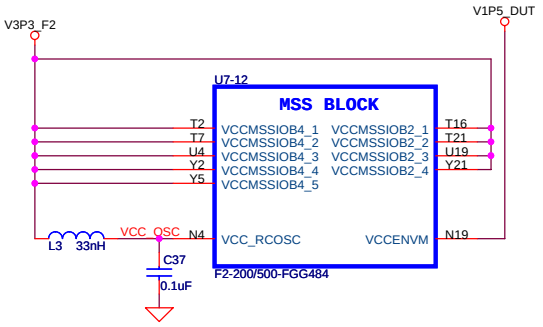
DIGITAL GROUND



DECOUPLING CAPACITORS



MSS BLOCK POWER SUPPLY



Actel

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Size B	Document Number DIGITAL PWR & GND	Rev F
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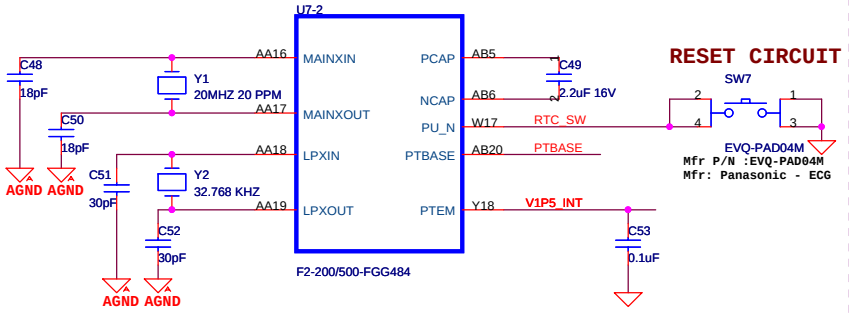
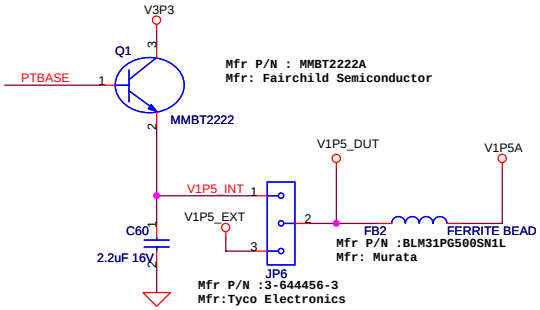
ANALOG SIGNAL PWR & GND

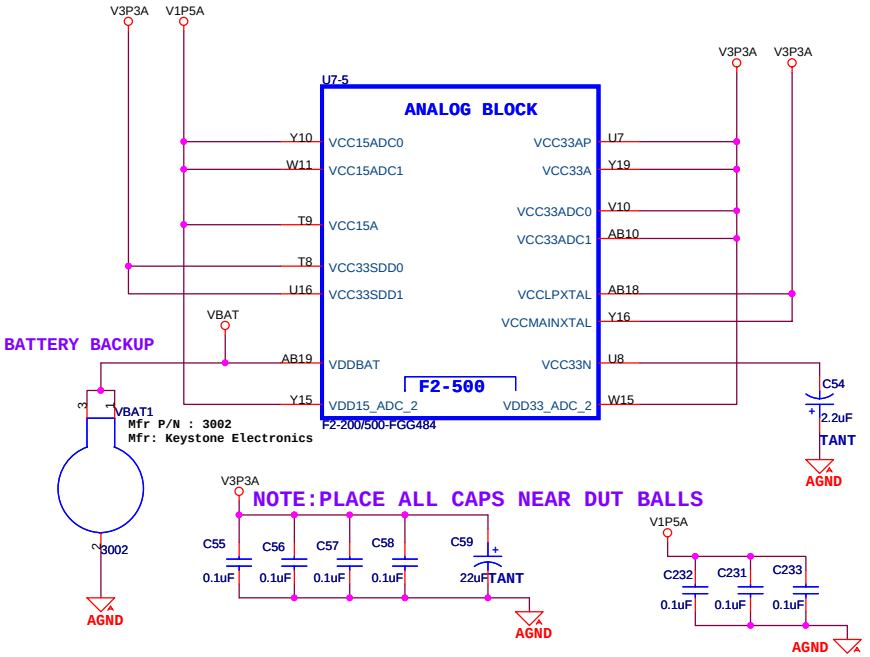
ANALOG BLOCK



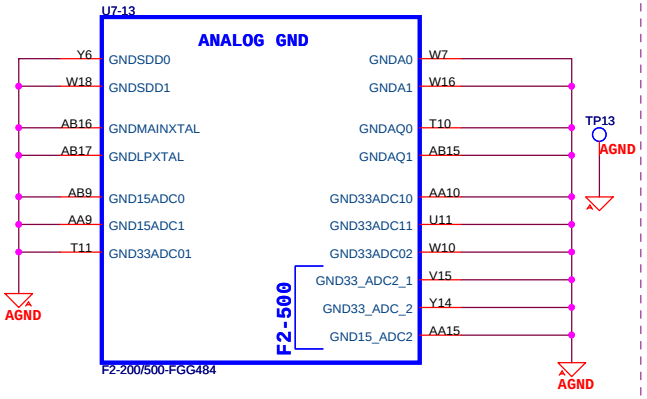
RESET CIRCUIT



ANALOG POWER SUPPLY



ANALOG GROUND



Actel

Title: A2F-DEV-KIT		
Size: B	Document Number: ANALOG SIGNAL PWR& GND	Rev: F
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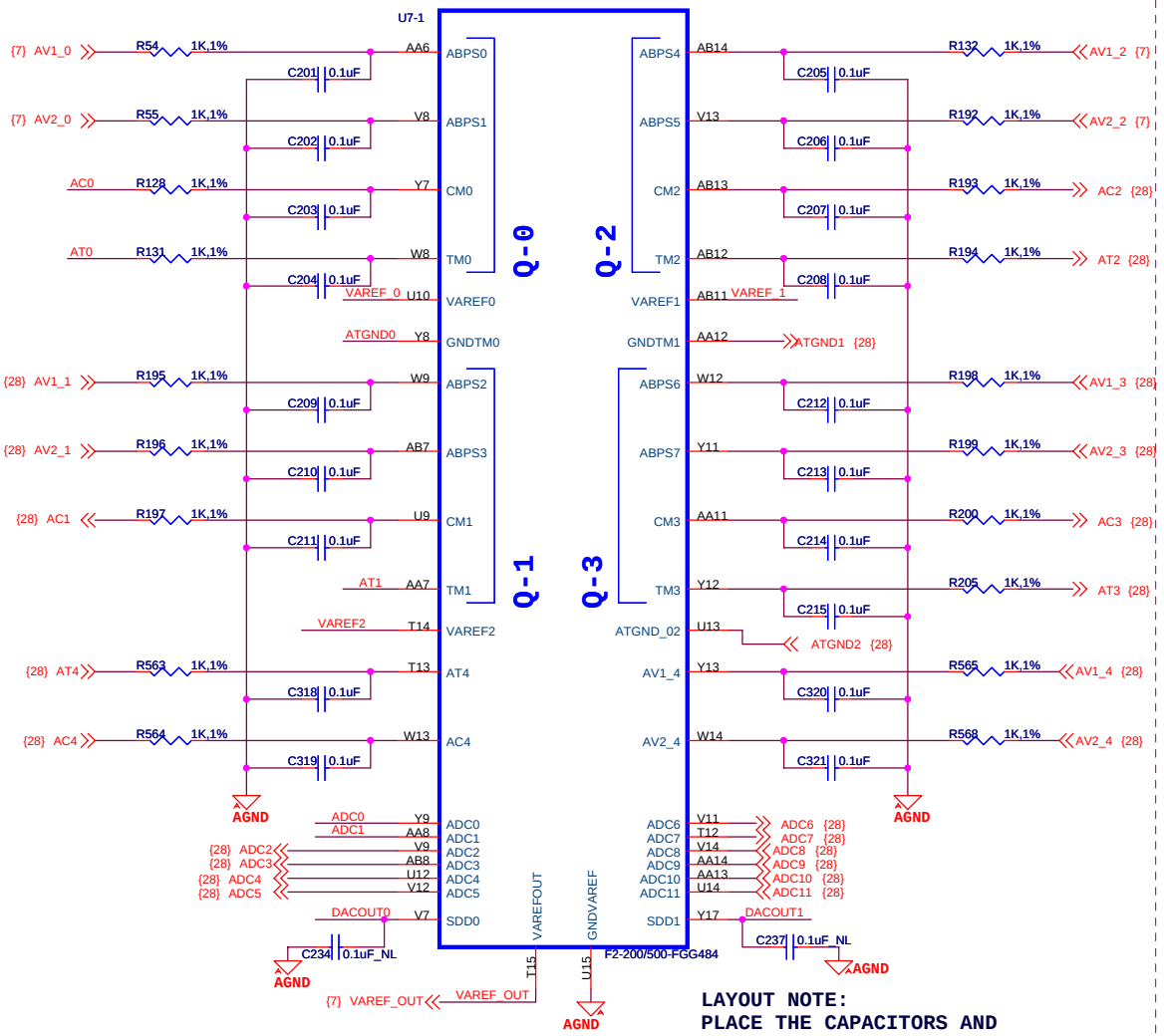
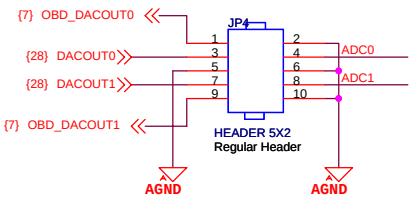
ANALOG SIGNAL



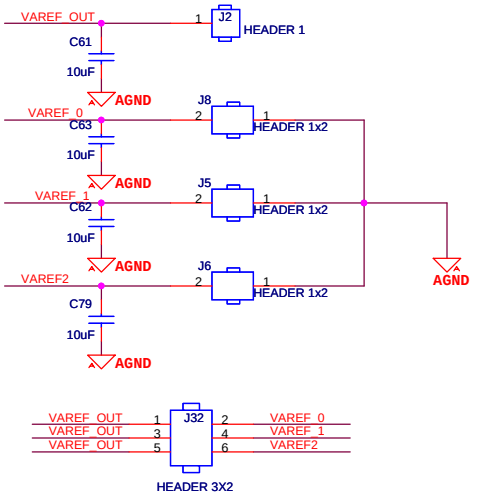
LAYOUT NOTE:
PLACE THE CAPACITORS AND RESISTORS IN "RC" CLOSE TO FPGA PIN

DEMO F2 COMPARATOR

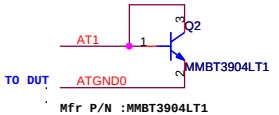


Place jumpers between pin 3&4 and 7&8

Input to OP-AMP	Shunt b/w JP4 pins	
U44	1	3
U51	7	9

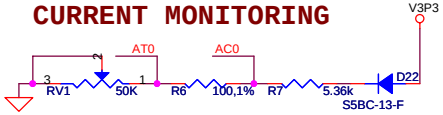


TEMP DIODE



Mfr P/N :MMBT3904LT1
Mfr:Infineon Technologies

CURRENT MONITORING



Actel

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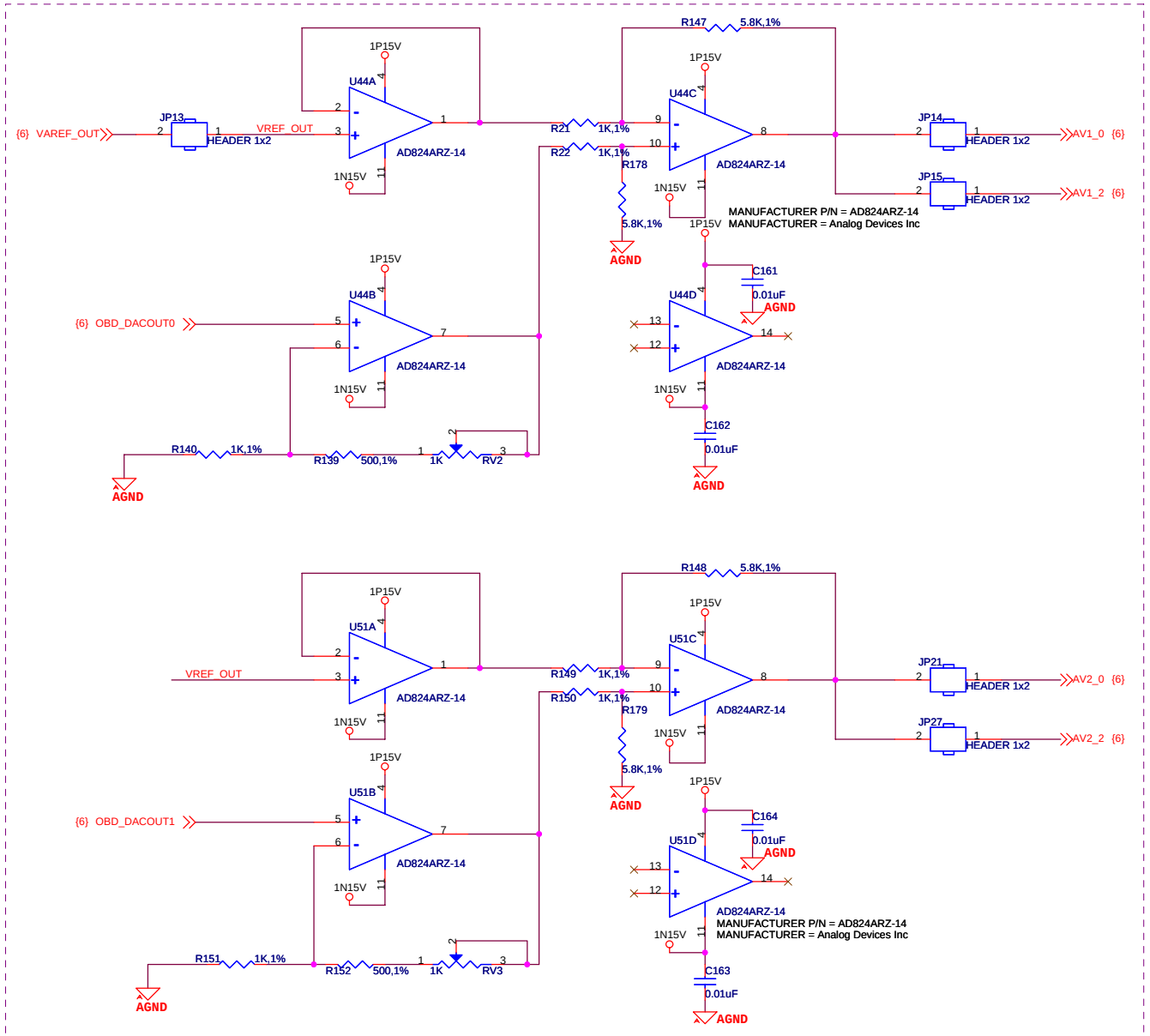
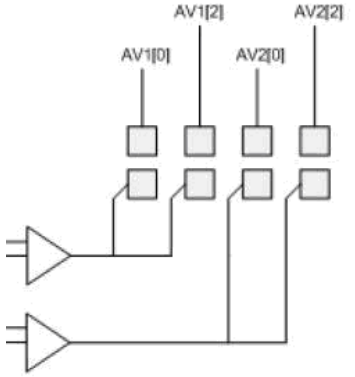
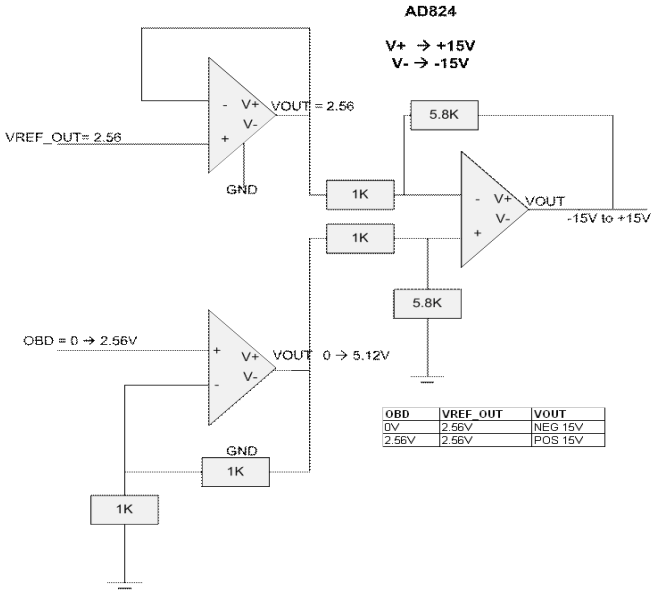
OBD_DACOUT







OBD	VREF_OUT	VOUT
0V	2.56V	NEG 15V
2.56V	2.56V	POS 15V

Actel

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Size: B	Document Number: OBD_DACOUT	Rev: F
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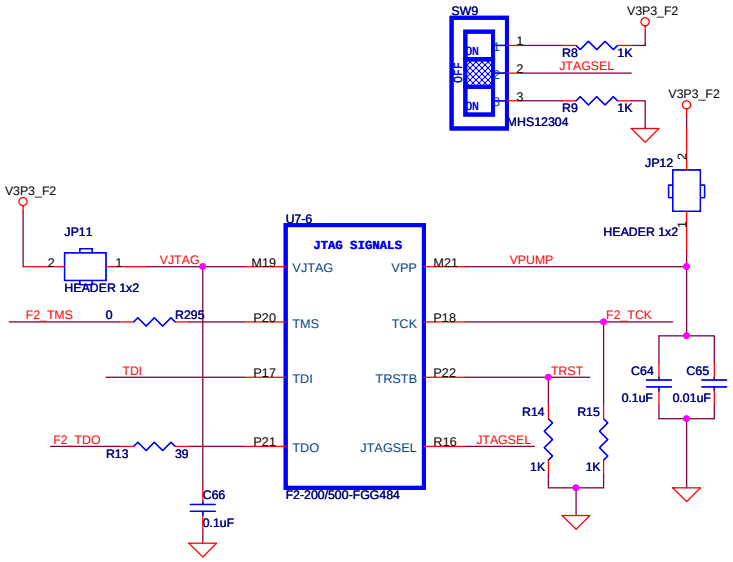
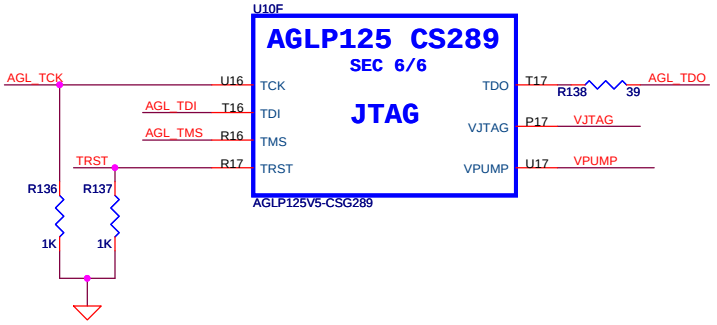
JTAG CHAIN PROGRAMMING

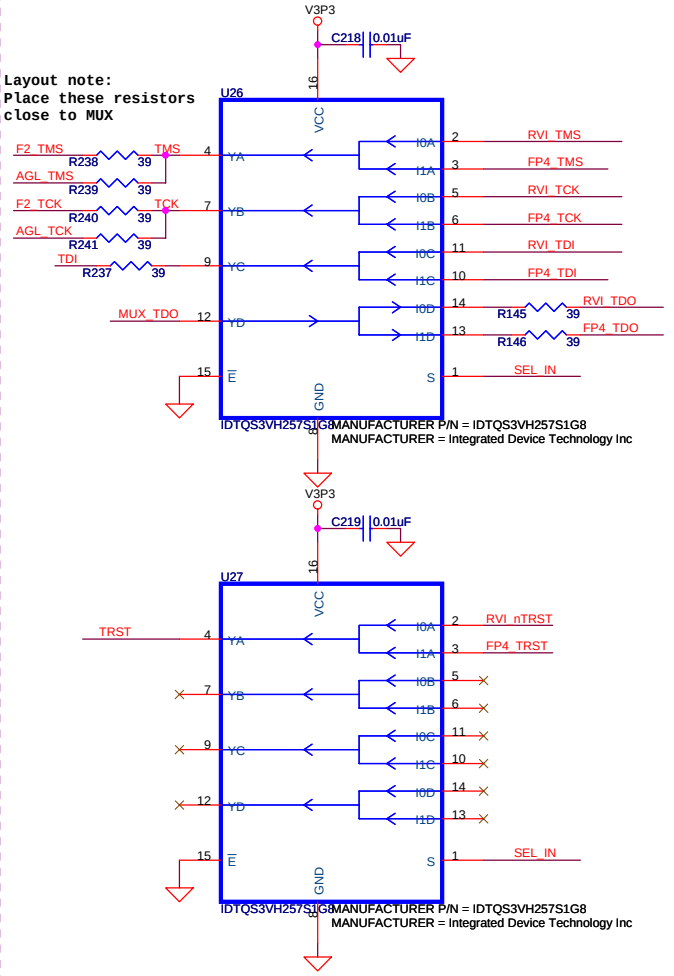
F2 JTAG



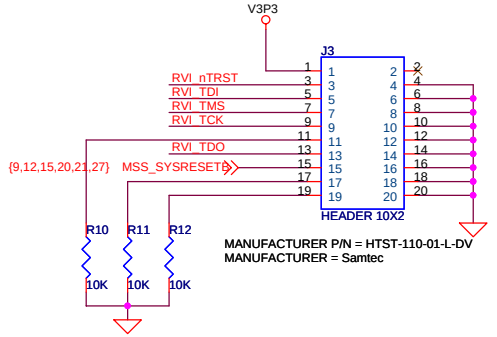
AGL JTAG



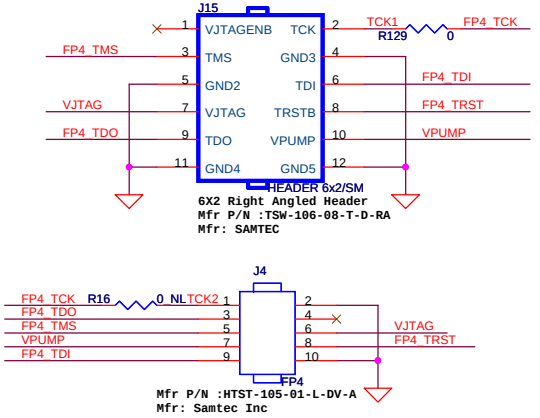
2:1 MUX/DEMUX



RVI HEADER



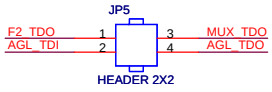
LC JTAG HEADER

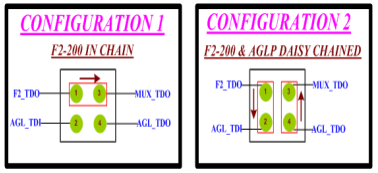


FP4 HEADER

R16 & R129 should be shared at "FP4_TCK" net side

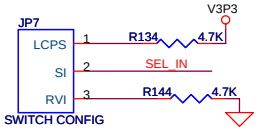
JTAG DEVICE OPTION





INPUT SELECTING OPTION

JTAG Config for MUX	Shunt b/w JP7 pins	
LCPS	1	2
RVI	2	3



Actel

Title	A2F-DEV-KIT	
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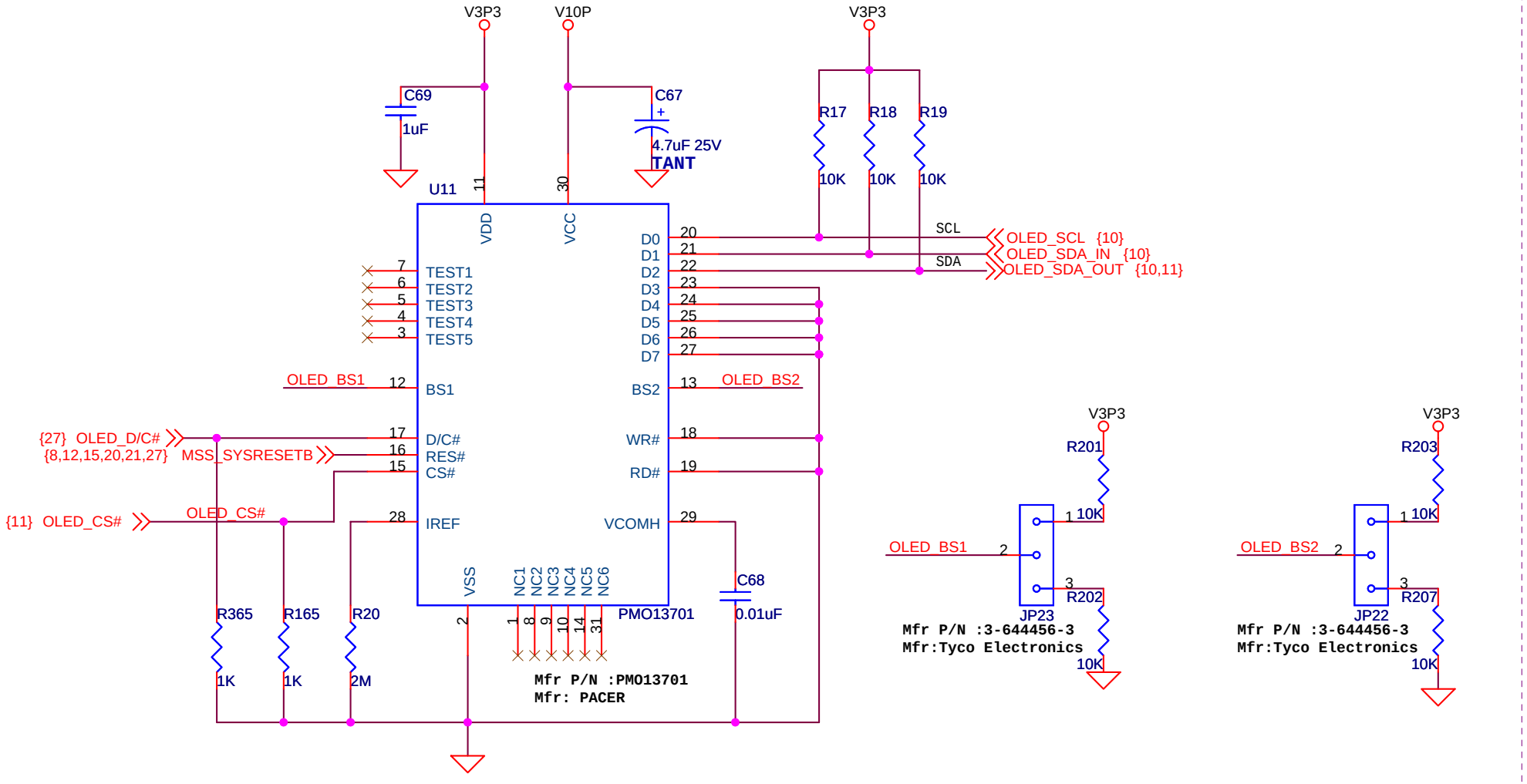
OLED DISPLAY



	I2C INTERFACE	SPI INTERFACE
BS1	1	0
BS2	0	0

Actel

Actel		
Title: A2F-DEV-KIT		
Size: A	Document Number: OLED DISPLAY	Rev: F
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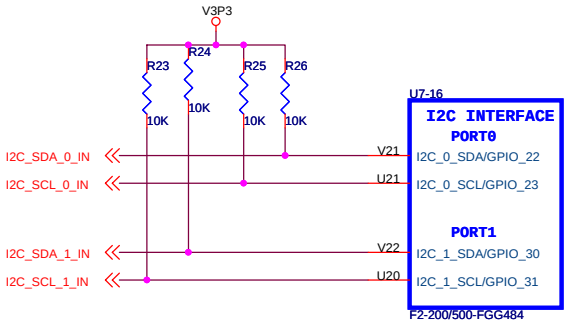
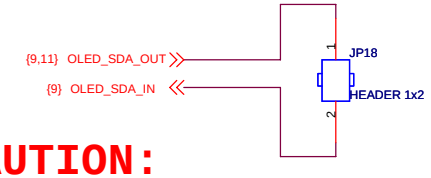
MSS BLOCK PAGE 1

Fusion2 MSS I2C Interface

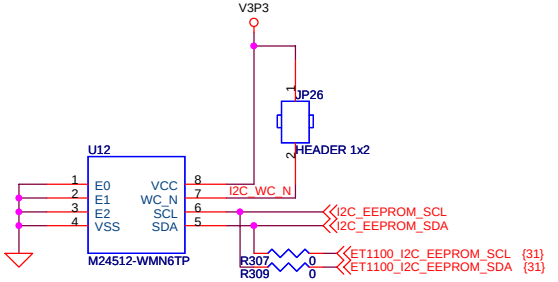




CAUTION:

Jumper should be added to this header JP18 only in I2C configuration Mode. Remove jumper in SPI Mode

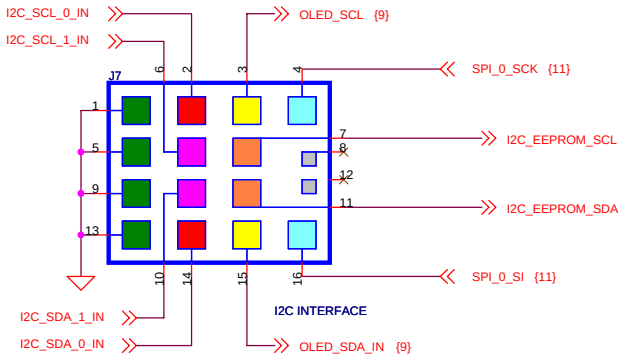
I2C EEPROM

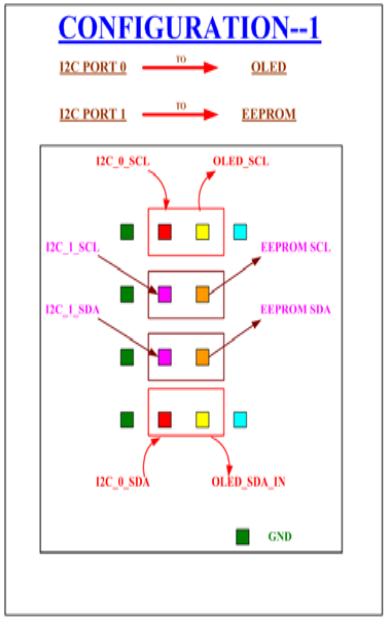


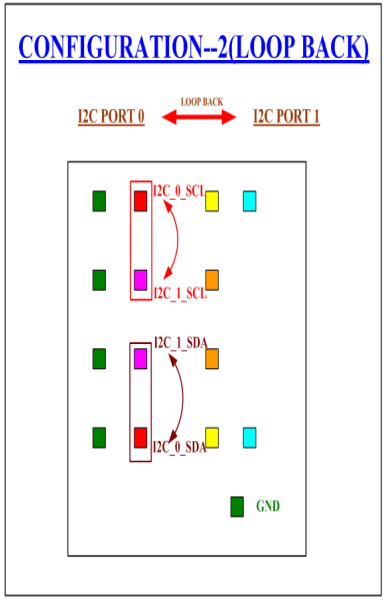
MANUFACTURER P/N = M24512-WMN6TP
MANUFACTURER = STMicroelectronics

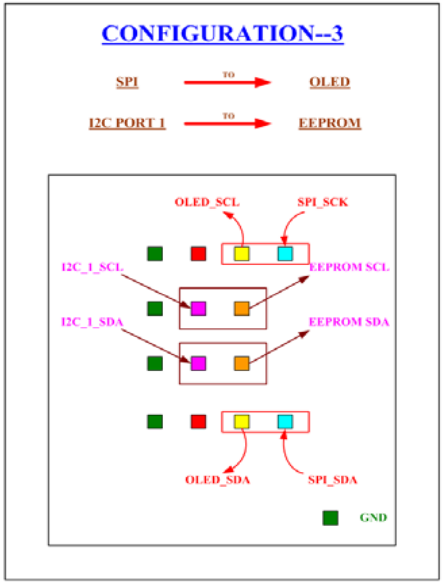
Device Select Code: " 0 0 0 "

SPI_0, I2C, EEPROM & OLED loop back









Actel

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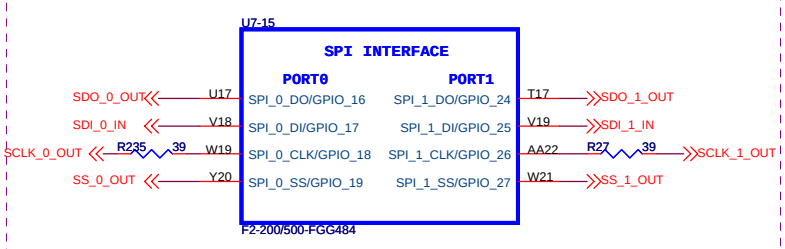
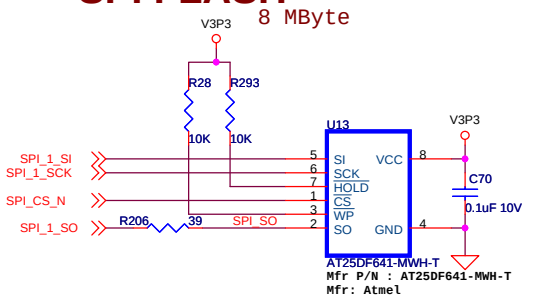
Fusion2 MSS SPI Interface

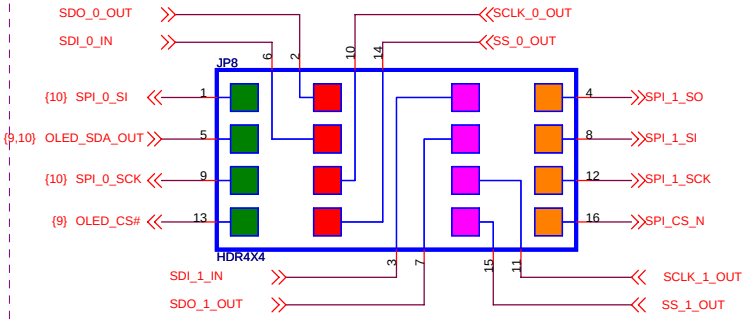


MSS BLOCK PAGE 2

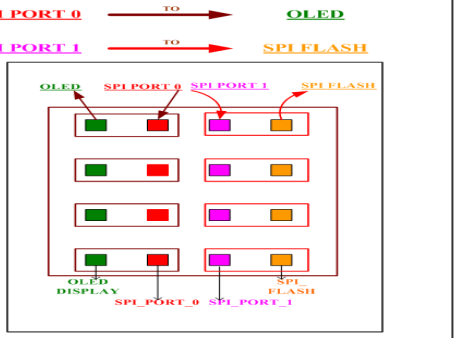
SPI FLASH



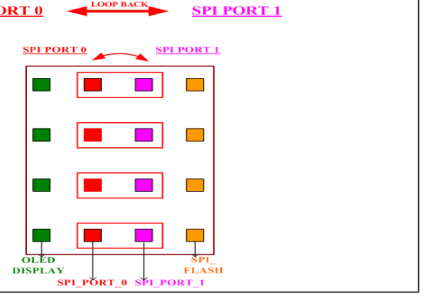
SPI loop back



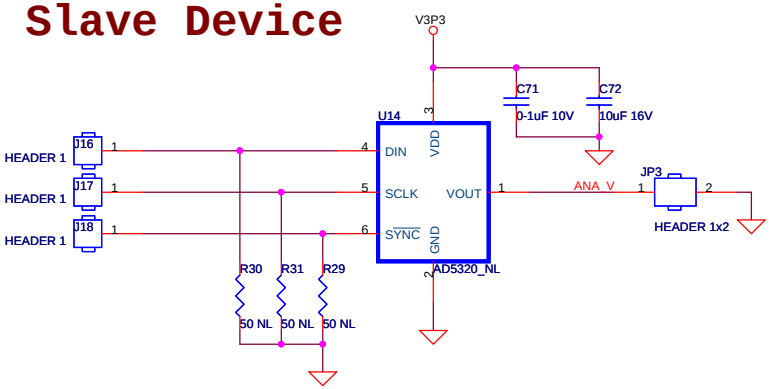
SPI CONFIGURATION--1



SPI CONFIGURATION--2(LOOP BACK)



Extra Slave Device



Actel

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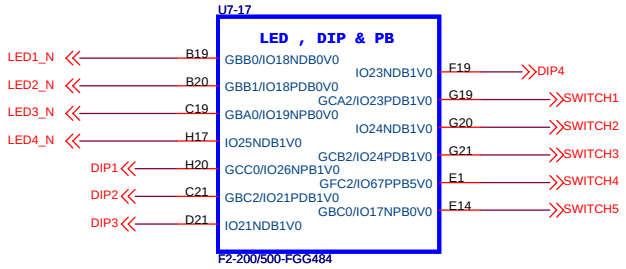
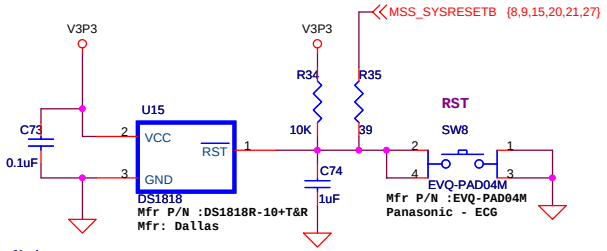
USER DEBUG LOGIC

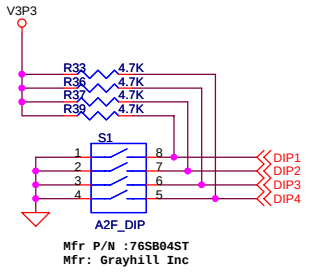


PUSH BUTTON SYSTEM RESET FOR DUT

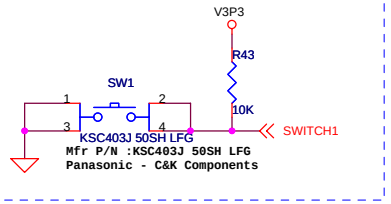


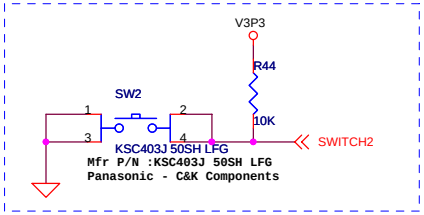
Notes;
R35 need to place at U15

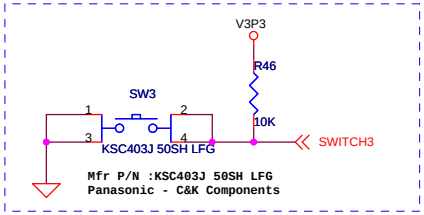
A2F_DIP

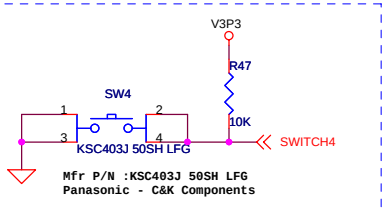


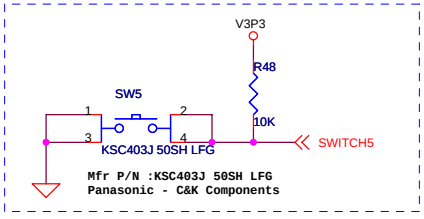
TEST & NAVIGATION SWITCHES



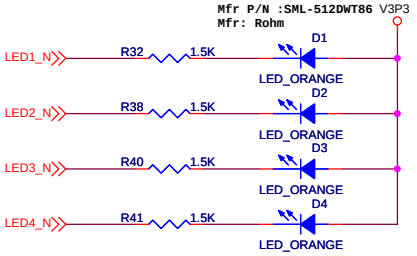






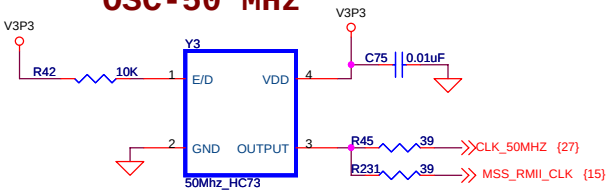


TEST LEDS



ACTIVE LOW

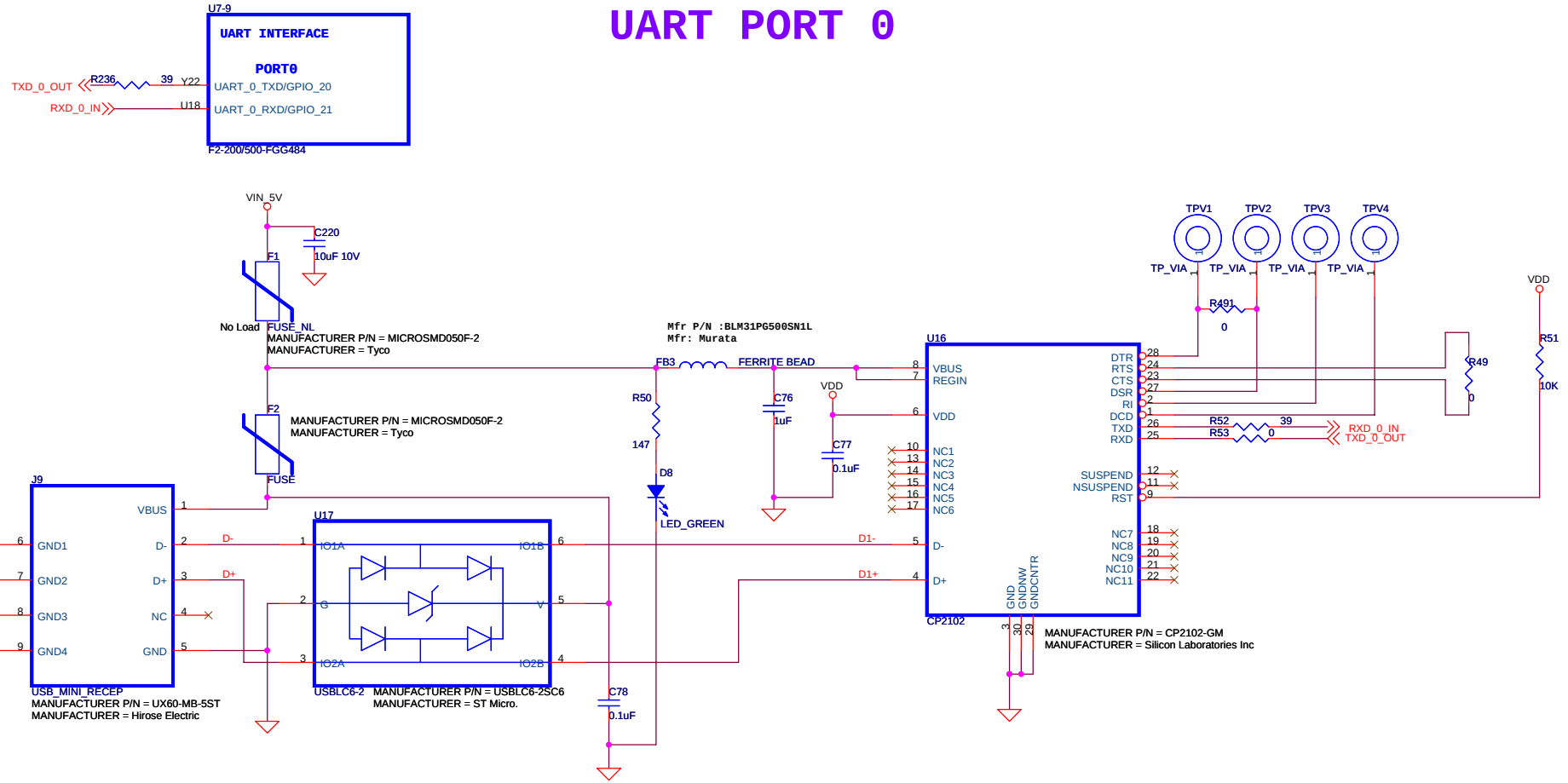
OSC-50 MHz



Actel

Title	A2F-DEV-KIT	
Size B	Document Number DEBUG CIRCUITS	Rev F
Date: Tuesday, March 30, 2010	Sheet 12 of 35	

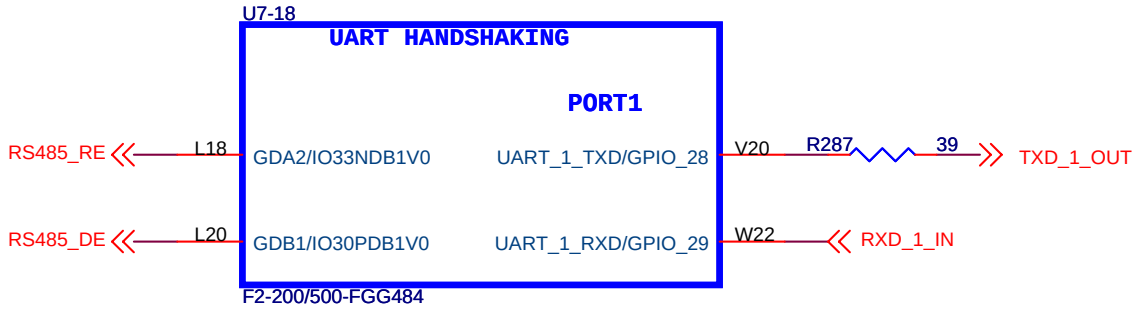
UART PORT 0

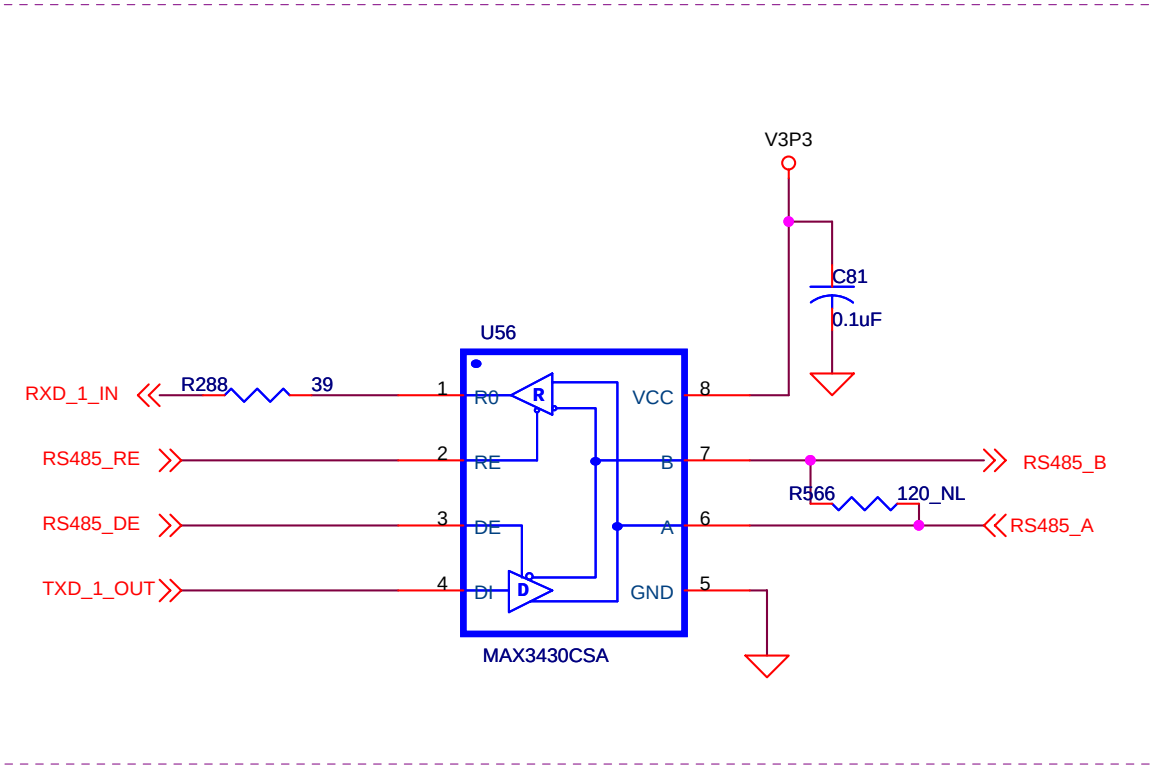


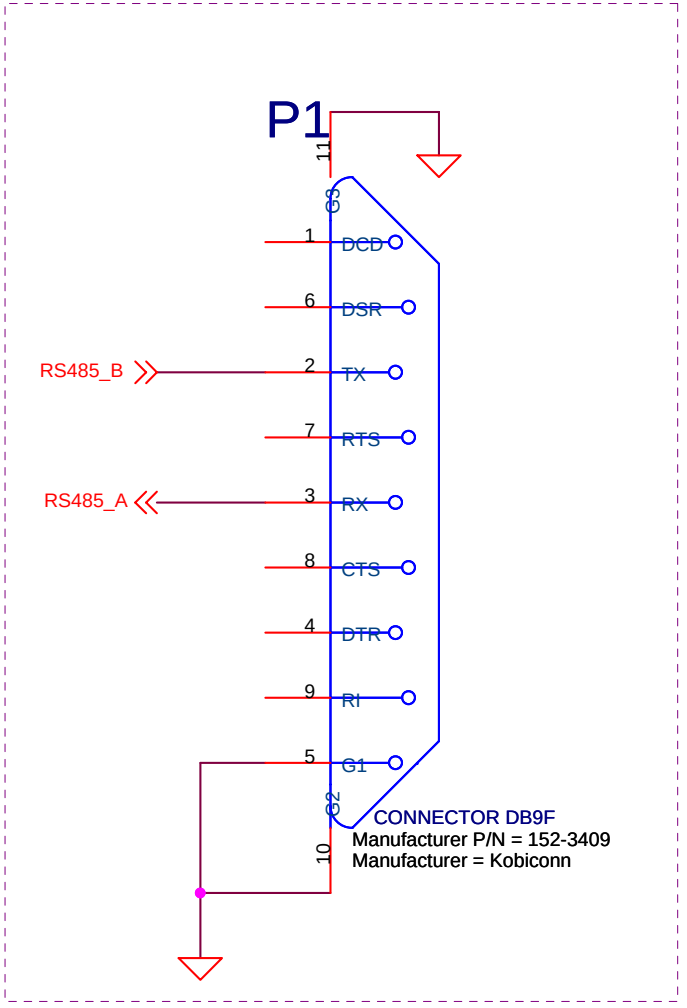
Actel

Title	A2F-DEV-KIT	
Size B	Document Number USB to UART CIRCUITS	Rev F
Date: Tuesday, March 30, 2010	Sheet 13 of 35	

UART PORT 1



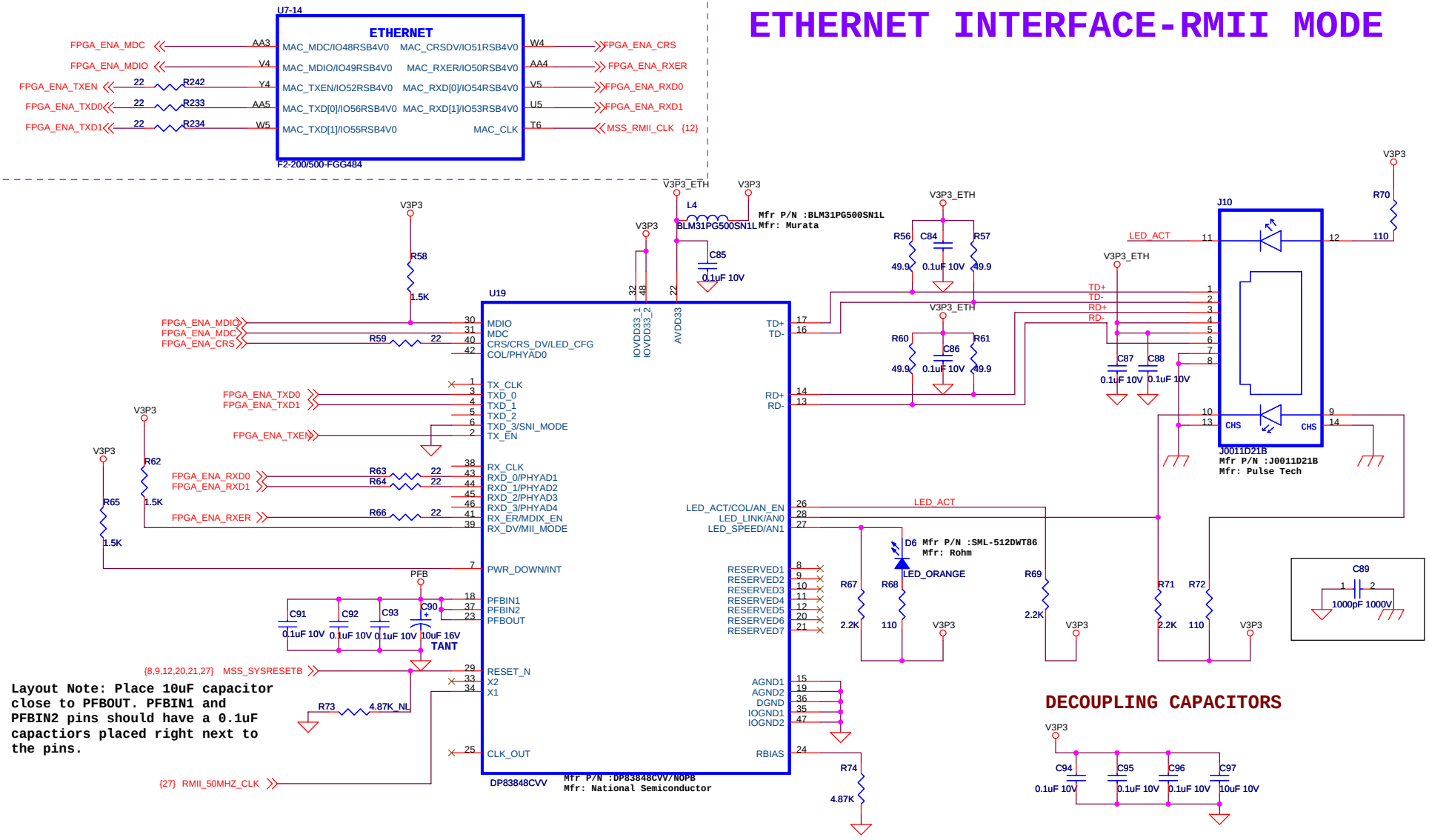




Actel

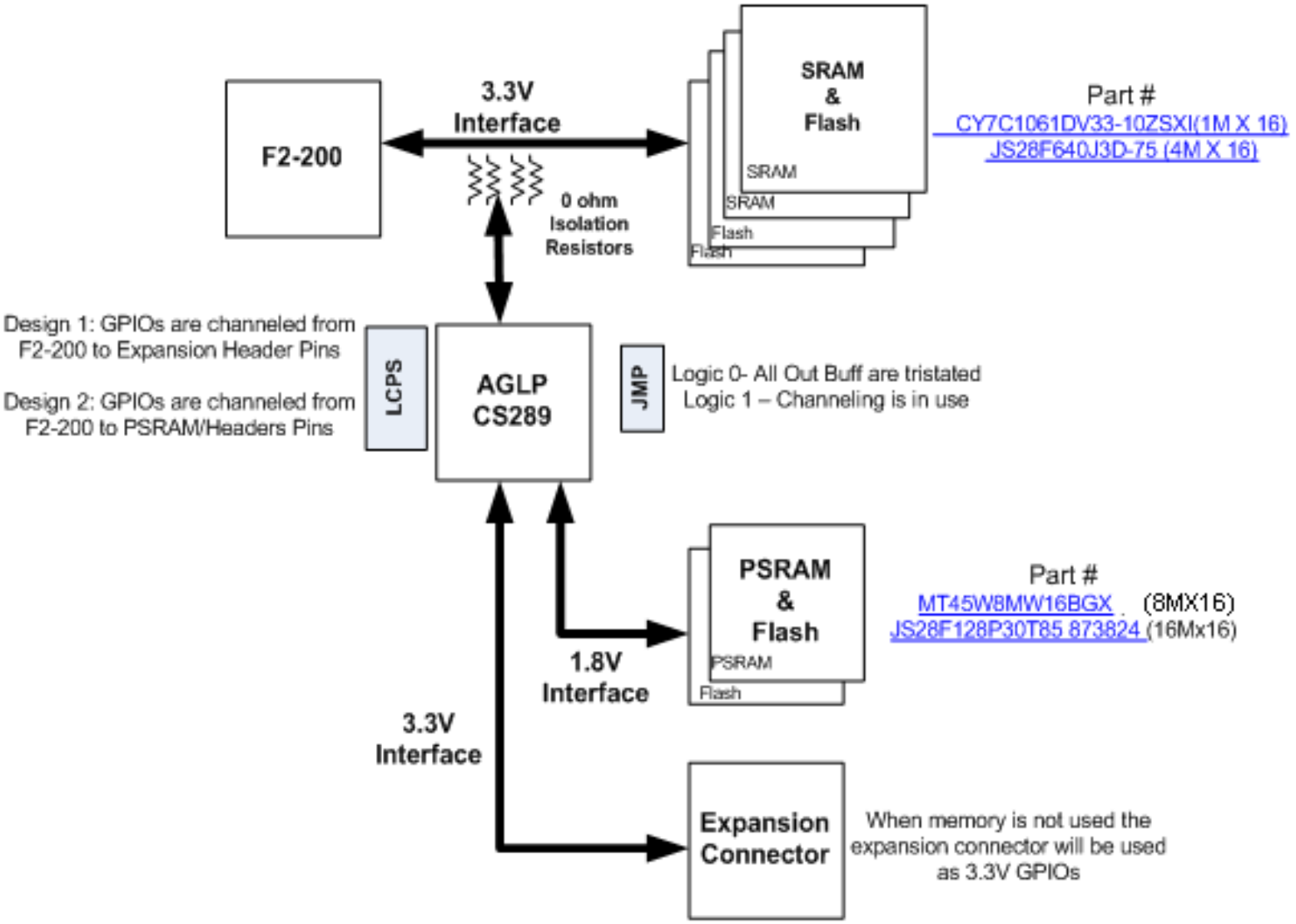
Title: A2F-DEV-KIT		
Size: A	Document Number: UART PORT 1	Rev: F
Date: Tuesday, March 30, 2010	Sheet 14 of 35	

ETHERNET INTERFACE-RMII MODE



Actel			
Title: A2F-DEV-KIT			
Size: B	Document Number: ETHERNET INTERFACE-RMII MODE		Rev: F
Date: Tuesday, March 30, 2010	Sheet 15 of 35		

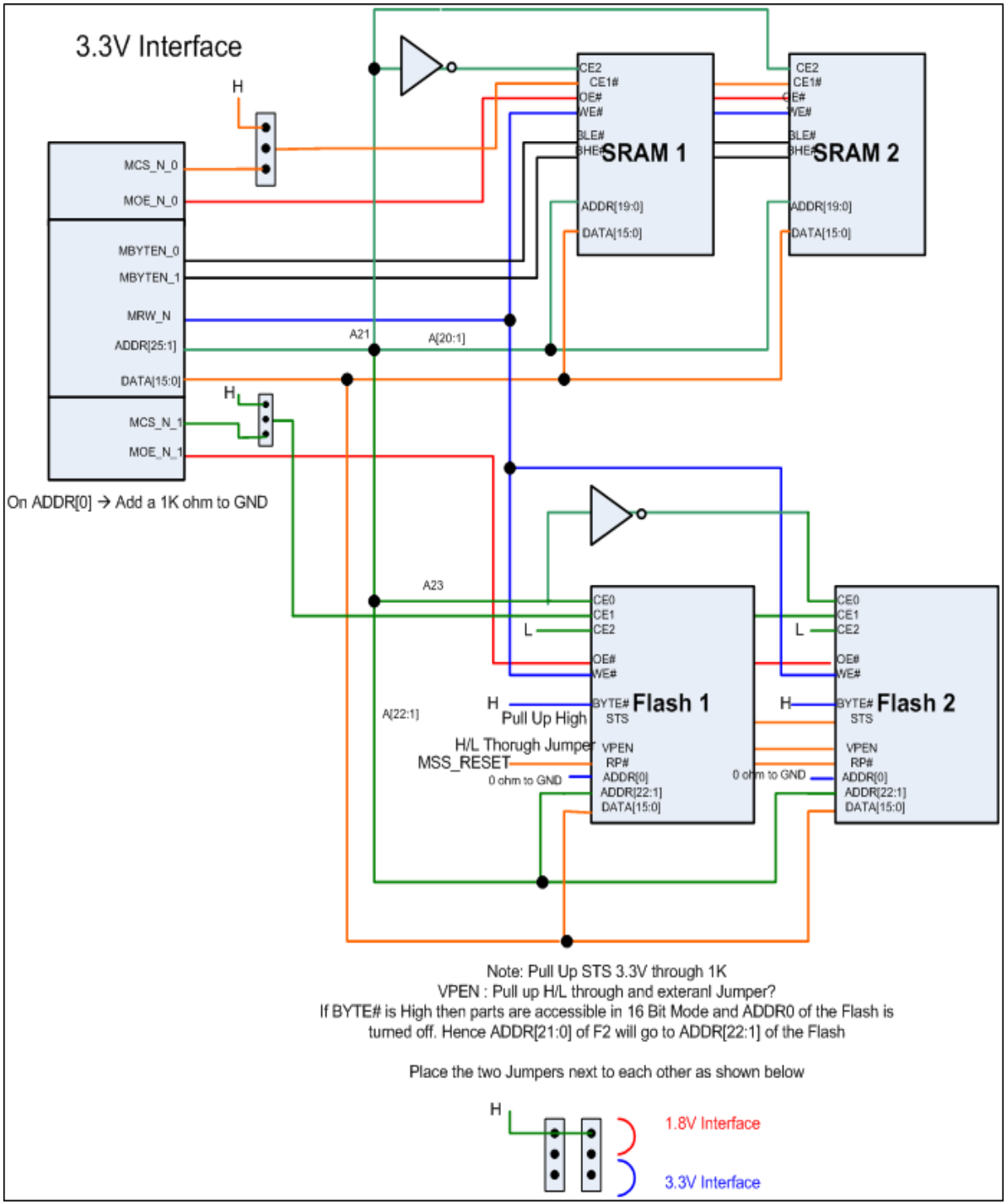
MEMORY SECTION



Actel

Actel		
Title: A2F-DEV-KIT		
Size: A	Document Number: MEMORY SECTION	Rev: F
Date: Tuesday, March 30, 2010	Sheet 16 of 35	

3.3V MEMORY SECTION



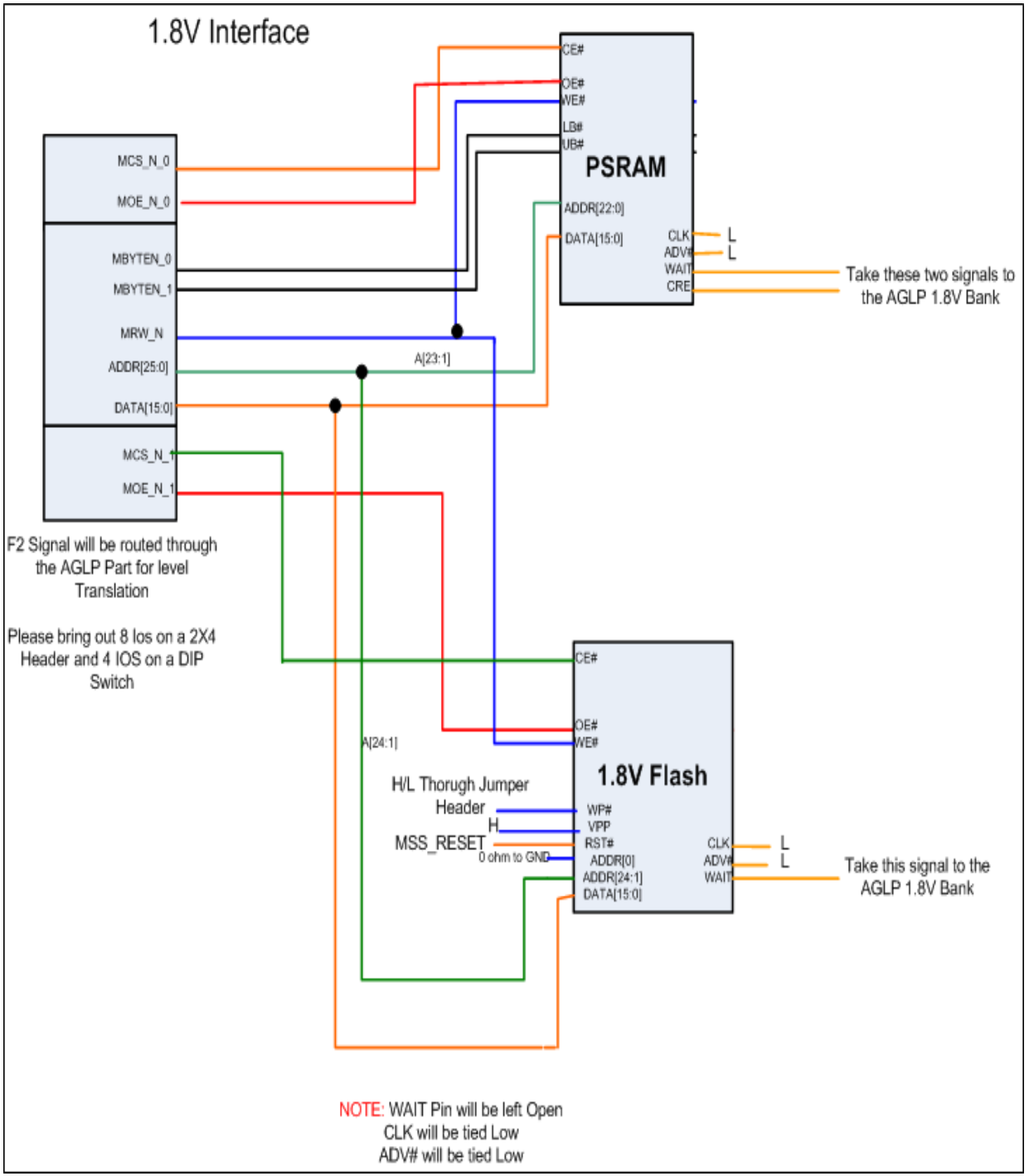
SRAM 1		SRAM 2					
CE1#	CE2	CE1#	CE2	Config			
0	1	0	0	SRAM 1 is Enabled and SRAM 2 is Disbaled			
0	0	0	1	SRAM 2 is Enabled and SRAM 1 is Disbaled			
1	1	1	0	SRAM 1,2 is disabled			
1	0	1	1	SRAM 1,2 is disabled			

Flash 1			Flash 2					
CE2	CE1	CE0	CE2	CE1	CE0	Config		
0	0	0	0	0	1	Flash 1 is Enable and Flash 2 is disabled		
0	0	1	0	0	0	Flash 2 is Enable and Flash 1 is disabled		
0	1	0	0	1	1	Flash 1,2 is disabled		
0	1	1	0	1	0	Flash 1,2 is disabled		

Actel

Actel		
Title: A2F-DEV-KIT		
Size: A	Document Number: 3.3V MEMORY SECTION	Rev: F
Date: Tuesday, March 30, 2010	Sheet 17 of 35	

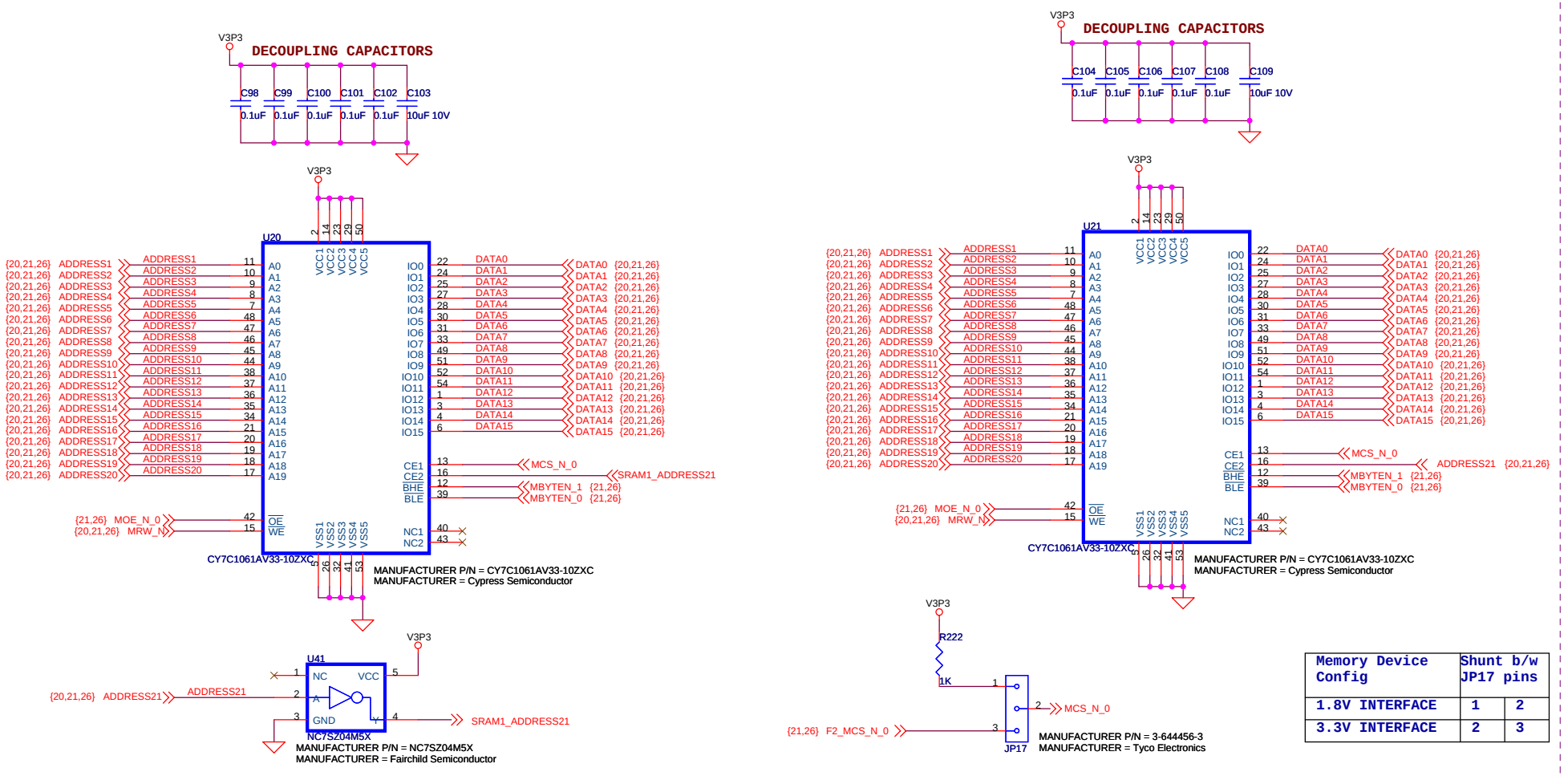
1.8V MEMORY SECTION



Actel

Title: A2F-DEV-KIT		
Size: A	Document Number: 1.8V MEMORY SECTION	Rev: F
Date: Tuesday, March 30, 2010	Sheet 18 of 35	

SRAM 16MBIT (1M x 16)

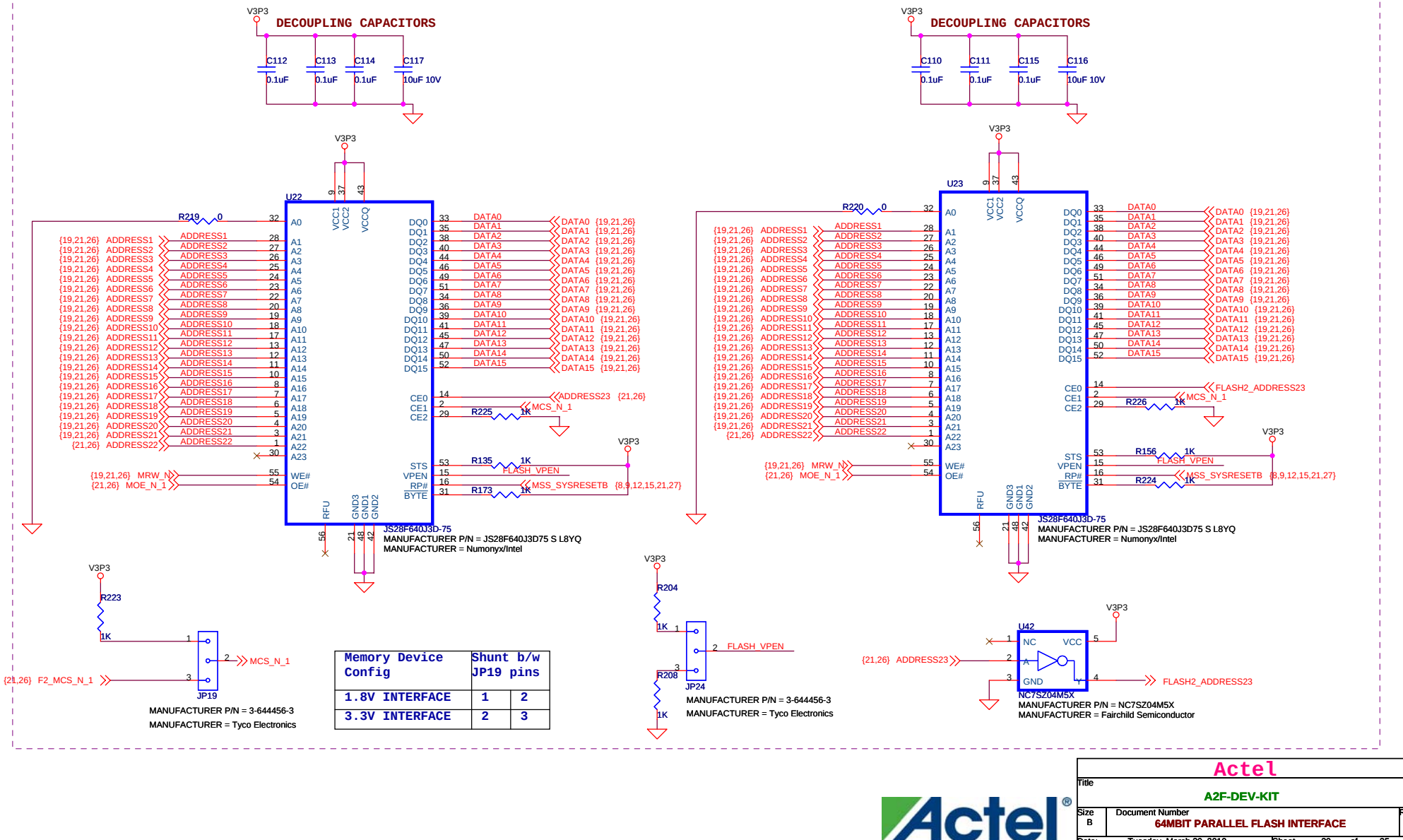


Memory Device Config	Shunt b/w JP17 pins	
1.8V INTERFACE	1	2
3.3V INTERFACE	2	3

Actel

Title: A2F-DEV-KIT		
Size: B	Document Number: SRAM 16MBIT (1M x 16)	Rev: F
Date: Tuesday, March 30, 2010	Sheet 19 of 35	

64MBIT PARALLEL FLASH INTERFACE



Memory Device Config	Shunt b/w JP19 pins	
1.8V INTERFACE	1	2
3.3V INTERFACE	2	3

Actel

Title: A2F-DEV-KIT		
Size: B	Document Number: 64MBIT PARALLEL FLASH INTERFACE	Rev: F
Date: Tuesday, March 30, 2010	Sheet 20 of 35	

3.3V MEMORY INTERFACE TO F2 DEVICE

U10C

AGLP125 CS289

SEC 3/6

BANK2

{19,20,26}	ADDRESS1	R82	0	AGLP_ADDRESS1	P14	IO108RSB2			
{19,20,26}	ADDRESS2	R75	0	AGLP_ADDRESS2	N14	IO109RSB2			
{19,20,26}	ADDRESS3	R76	0	AGLP_ADDRESS3	R15	IO110RSB2			
{19,20,26}	ADDRESS4	R77	0	AGLP_ADDRESS4	N12	IO111RSB2			
{19,20,26}	ADDRESS5	R78	0	AGLP_ADDRESS5	P12	IO112RSB2			
{19,20,26}	ADDRESS6	R80	0	AGLP_ADDRESS6	M12	IO113RSB2			
{19,20,26}	ADDRESS7	R81	0	AGLP_ADDRESS7	R14	IO114RSB2			
{19,20,26}	ADDRESS8	R89	0	AGLP_ADDRESS8	T15	IO115RSB2			
{19,20,26}	ADDRESS9	R91	0	AGLP_ADDRESS9	R13	IO116RSB2			
{19,20,26}	ADDRESS10	R92	0	AGLP_ADDRESS10	U15	IO117RSB2			
{19,20,26}	ADDRESS11	R93	0	AGLP_ADDRESS11	R12	IO118RSB2			
{19,20,26}	ADDRESS12	R94	0	AGLP_ADDRESS12	N11	IO119RSB2			
{19,20,26}	ADDRESS13	R95	0	AGLP_ADDRESS13	U14	IO120RSB2			
{19,20,26}	ADDRESS14	R96	0	AGLP_ADDRESS14	M11	IO121RSB2			
{19,20,26}	ADDRESS15	R97	0	AGLP_ADDRESS15	T13	IO122RSB2			
{19,20,26}	ADDRESS16	R98	0	AGLP_ADDRESS16	U13	IO123RSB2			
{19,20,26}	ADDRESS17	R99	0	AGLP_ADDRESS17	T12	IO124RSB2			
{19,20,26}	ADDRESS18	R100	0	AGLP_ADDRESS18	P10	IO125RSB2			
{19,20,26}	ADDRESS19	R101	0	AGLP_ADDRESS19	P11	IO126RSB2			
{19,20,26}	ADDRESS20	R102	0	AGLP_ADDRESS20	T11	IO127RSB2			
{19,20,26}	ADDRESS21	R103	0	AGLP_ADDRESS21	M10	IO128RSB2			
{20,26}	ADDRESS22	R104	0	AGLP_ADDRESS22	U11	IO129RSB2			
{20,26}	ADDRESS23	R105	0	AGLP_ADDRESS23	R10	IO130RSB2			
{19,20,26}	DATA0	R106	0	AGLP_DATA0	T10	IO131RSB2			
{19,20,26}	DATA1	R107	0	AGLP_DATA1	P9	IO132RSB2			
{19,20,26}	DATA2	R108	0	AGLP_DATA2	U10	IO133RSB2			
{19,20,26}	DATA3	R109	0	AGLP_DATA3	R9	IO134RSB2			
{19,20,26}	DATA4	R110	0	AGLP_DATA4	M9	IO135RSB2			
{19,20,26}	DATA5	R112	0	AGLP_DATA5	U9	IO136RSB2			
{19,20,26}	DATA6	R113	0	AGLP_DATA6	N9	IO137RSB2			
{19,20,26}	DATA7	R114	0	AGLP_DATA7	U8	IO138RSB2			

					T8	IO139RSB2	AGLP_DATA8	R83	0 DATA8 {19,20,26}
					T7	IO140RSB2	AGLP_DATA9	R84	0 DATA9 {19,20,26}
					R8	IO141RSB2	AGLP_DATA10	R85	0 DATA10 {19,20,26}
					U6	IO142RSB2	AGLP_DATA11	R86	0 DATA11 {19,20,26}
					T6	IO143RSB2	AGLP_DATA12	R79	0 DATA12 {19,20,26}
					N8	IO144RSB2	AGLP_DATA13	R87	0 DATA13 {19,20,26}
					R7	IO145RSB2	AGLP_DATA14	R88	0 DATA14 {19,20,26}
					U5	IO146RSB2	AGLP_DATA15	R90	0 DATA15 {19,20,26}
					T5	IO147RSB2			
					N7	IO148RSB2	AGLP_ADDRESS24	R174	0 ADDRESS24 {26}
					U4	IO149RSB2	AGLP_ADDRESS25	R175	0 ADDRESS25 {26}
					R5	IO150RSB2	R166	0	MOE_N_0 {19,26}
					U3	IO151RSB2	R167	0	MOE_N_1 {20,26}
					P7	IO152RSB2	R168	0	MBYTEN_0 {19,26}
					T3	IO153RSB2	R169	0	MBYTEN_1 {19,26}
					P6	IO154RSB2	R170	0	F2_MCS_N_0 {19,26}
					R4	IO155RSB2	R171	0	F2_MCS_N_1 {20,26}
					N6	IO156RSB2	R172	0	MRW_N {19,20,26}
					P5	IO157RSB2	R176	0	MSS_SYSRESETB {8,9,12,15,20,27}
					R3	IO158RSB2	AGLP_3.3V_SIG1		
					M7	IO159RSB2	AGLP_3.3V_SIG2		
					P4	IO160RSB2	AGLP_3.3V_SIG3		
					M8	IO161RSB2	AGLP_3.3V_SIG4		
					P15	GDA2/IO105RSB2	R177	0	EM_CLK {26}
					N13	GDB2/IO106RSB2	AGLP_3.3V_DIP1		
					P16	GDC2/IO107RSB2	AGLP_3.3V_DIP2		
					R2	GEA2/IO164RSB2	AGLP_3.3V_DIP3		
					U1	FF/GEB2/IO163RSB2	F*F		
					T2	GEC2/IO162RSB2	AGLP_3.3V_DIP4		

AGLP125V5-CSG289

V3P3 R111 10K

JP16

R115 10K

J20

AGLP_3.3V_SIG1 AGLP_3.3V_SIG2 — 1 2 3 4 — AGLP_3.3V_SIG3 AGLP_3.3V_SIG4

HEADER 2X2

AGLP_DIP

V3P3

R158 4.7K
R161 4.7K
R163 4.7K
R164 4.7K

S2

1 2 3 4 — 8 7 6 5 — AGLP_3.3V_DIP1 AGLP_3.3V_DIP2 AGLP_3.3V_DIP3 AGLP_3.3V_DIP4

AGLP_DIP Mfr P/N:76SB04ST Mfr: GrayhillInc

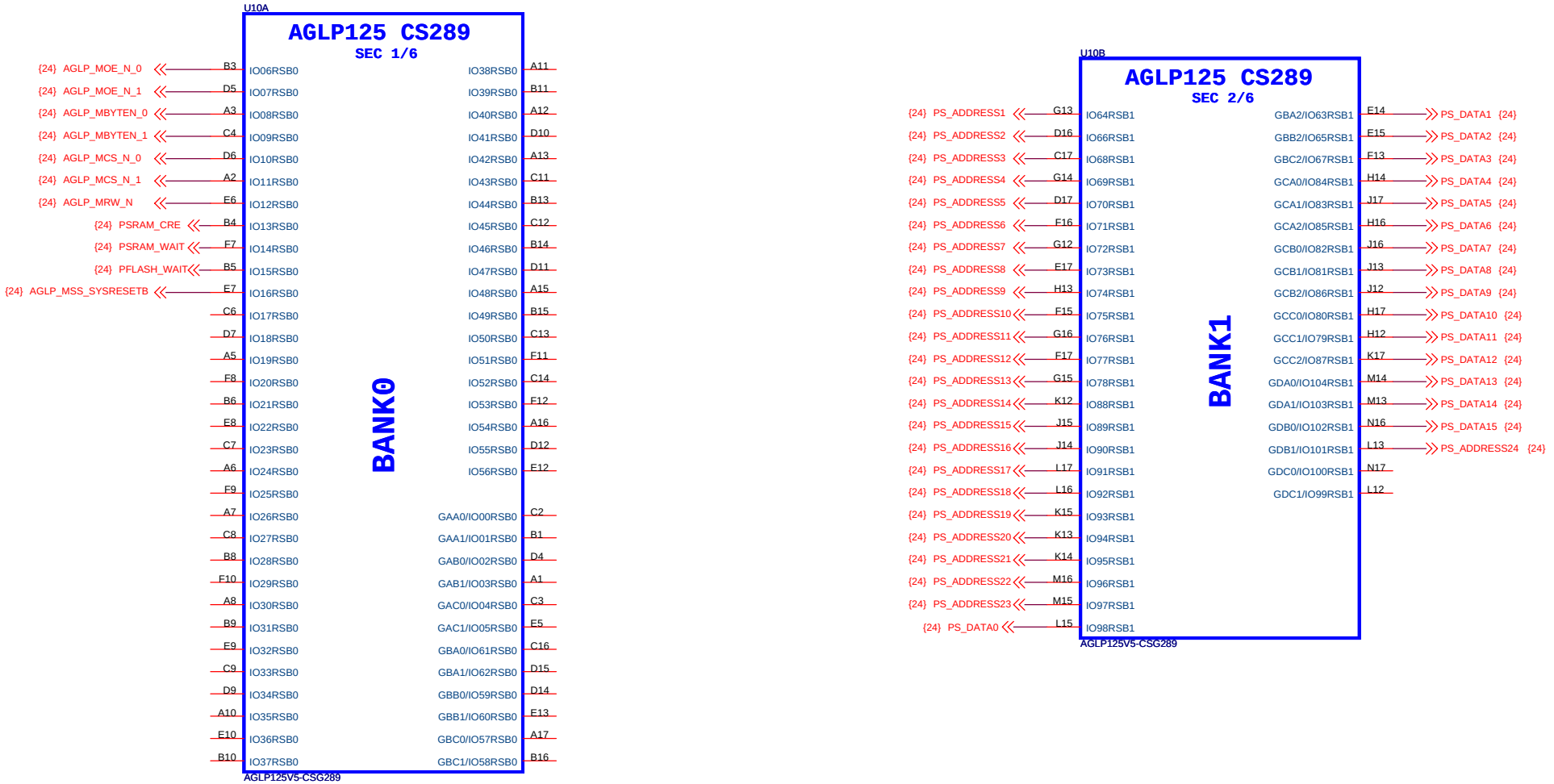
TERMINATION RESISTORS

AGLP_ADDRESS1	R130	50 NL	AGLP_DATA0	R279	50 NL
AGLP_ADDRESS2	R221	50 NL	AGLP_DATA1	R264	50 NL
AGLP_ADDRESS3	R243	50 NL	AGLP_DATA2	R265	50 NL
AGLP_ADDRESS4	R244	50 NL	AGLP_DATA3	R266	50 NL
AGLP_ADDRESS5	R245	50 NL	AGLP_DATA4	R267	50 NL
AGLP_ADDRESS6	R246	50 NL	AGLP_DATA5	R268	50 NL
AGLP_ADDRESS7	R247	50 NL	AGLP_DATA6	R269	50 NL
AGLP_ADDRESS8	R248	50 NL	AGLP_DATA7	R270	50 NL
AGLP_ADDRESS9	R249	50 NL	AGLP_DATA8	R271	50 NL
AGLP_ADDRESS10	R250	50 NL	AGLP_DATA9	R272	50 NL
AGLP_ADDRESS11	R251	50 NL	AGLP_DATA10	R273	50 NL
AGLP_ADDRESS12	R252	50 NL	AGLP_DATA11	R274	50 NL
AGLP_ADDRESS13	R253	50 NL	AGLP_DATA12	R275	50 NL
AGLP_ADDRESS14	R254	50 NL	AGLP_DATA13	R276	50 NL
AGLP_ADDRESS15	R255	50 NL	AGLP_DATA14	R277	50 NL
AGLP_ADDRESS16	R256	50 NL	AGLP_DATA15	R278	50 NL
AGLP_ADDRESS17	R257	50 NL			
AGLP_ADDRESS18	R258	50 NL			
AGLP_ADDRESS19	R259	50 NL			
AGLP_ADDRESS20	R260	50 NL			
AGLP_ADDRESS21	R261	50 NL			
AGLP_ADDRESS22	R262	50 NL			
AGLP_ADDRESS23	R263	50 NL			
AGLP_ADDRESS24	R294	50 NL			
AGLP_ADDRESS25	R303	50 NL			

Actel

Actel		
Title	A2F-DEV-KIT	
Size B	Document Number 3.3V MEMORY INTERFACE TO F2 DEVICE	Rev F
Date: Tuesday, March 30, 2010	Sheet 21 of 35	

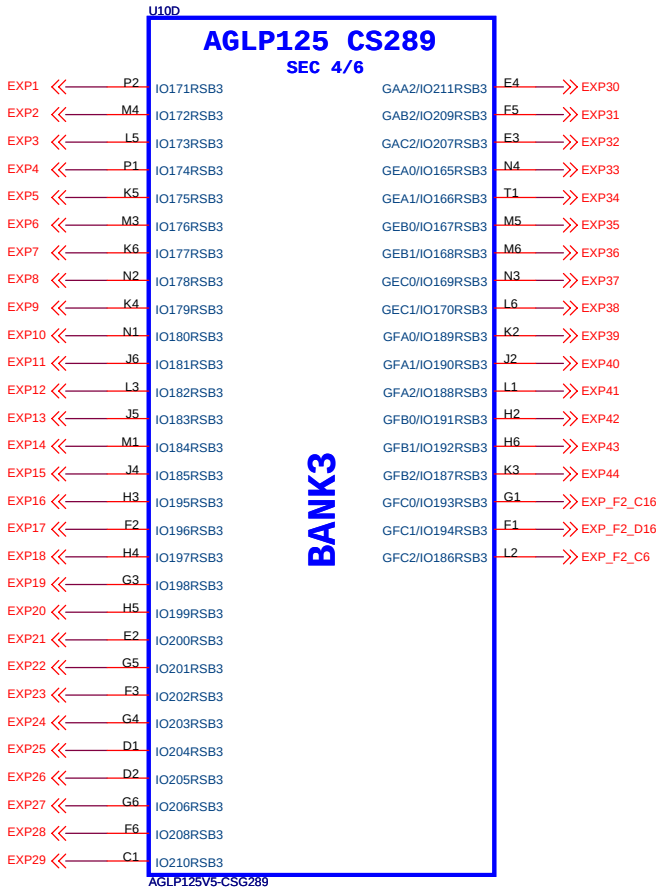
1.8V MEMORY INTERFACE TO PSRAM/FLASH DEVICE



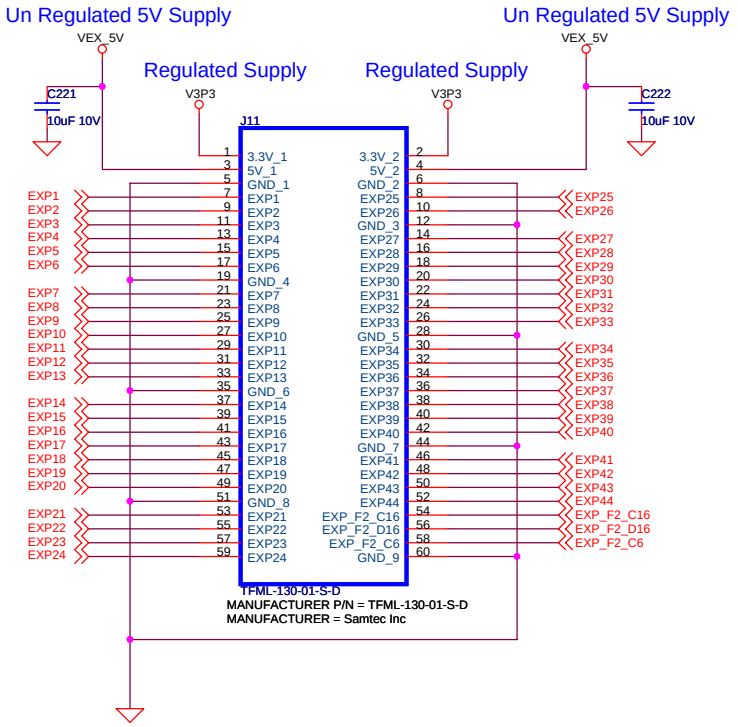
Actel			
Title: A2F-DEV-KIT			
Size: B	Document Number: 1.8V Memory Interface to PSRAM/Flash device		Rev: F
Date: Tuesday, March 30, 2010	Sheet 22 of 35		

AGL 125 & EXPANSION HEADER

AGL 125 CS289 IO



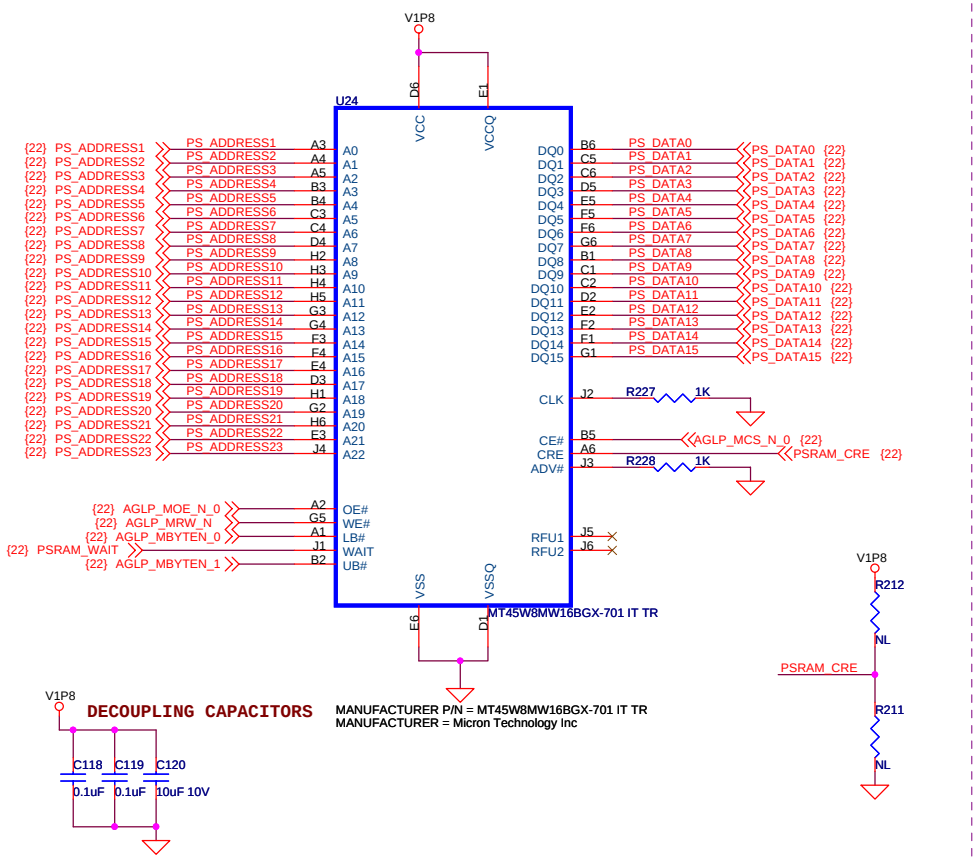
A2F EMC EXPANSION HEADER



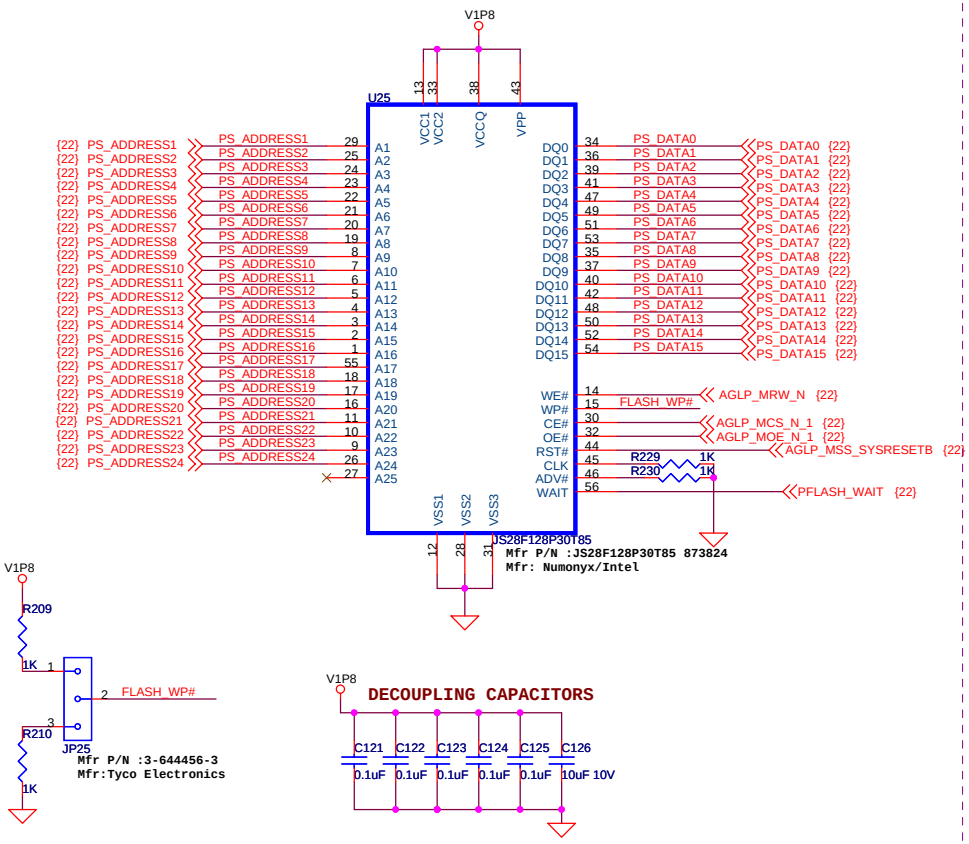
Actel

Actel		
Title: A2F-DEV-KIT		
Size: B	Document Number: AGL 125 & EXPANSION HEADER	Rev: F
Date: Tuesday, March 30, 2010	Sheet 23 of 35	

PSRAM 128MBIT (8M x 16)

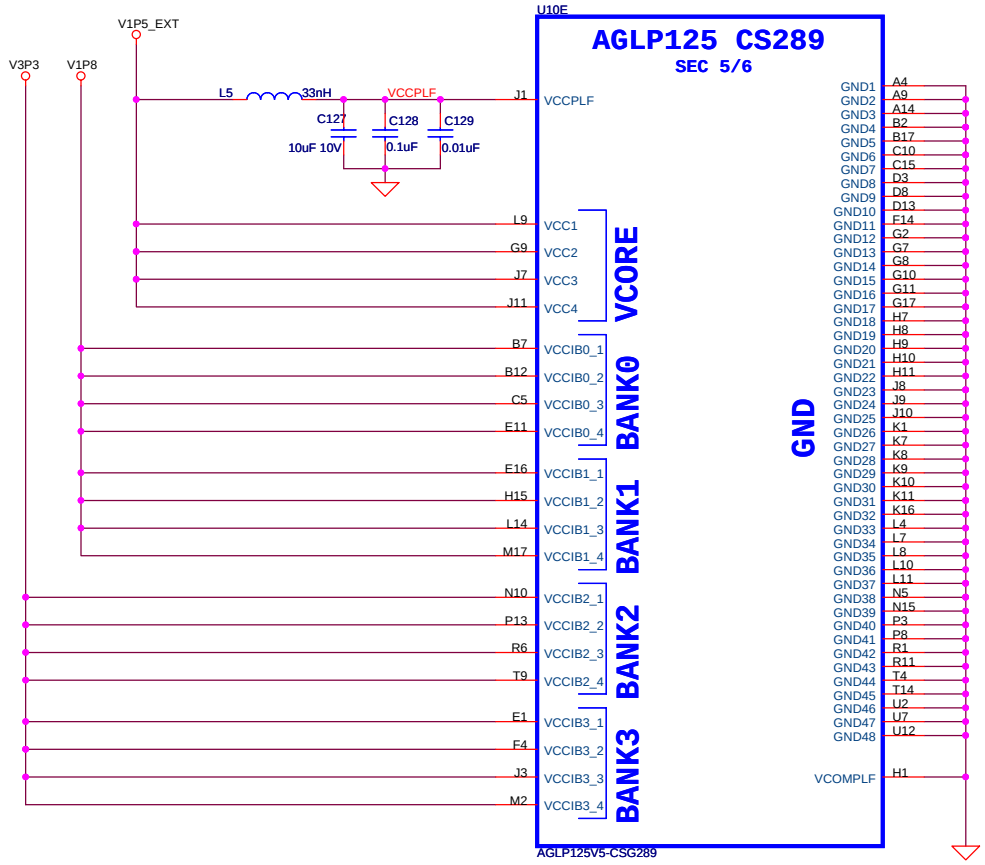


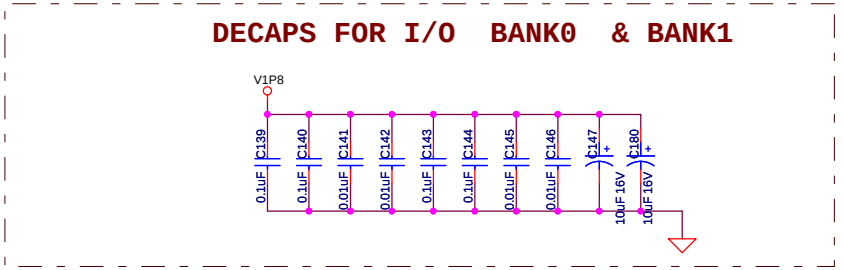
FLASH 128MBIT (8M x 16)

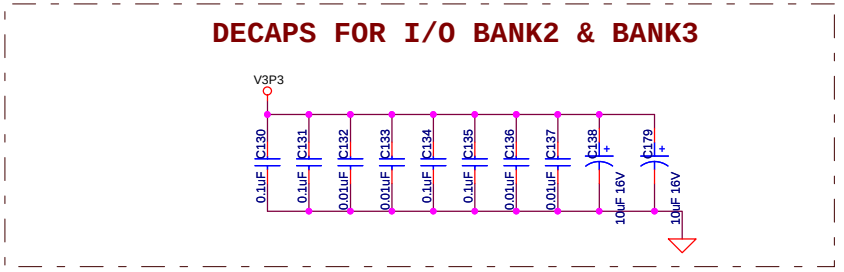


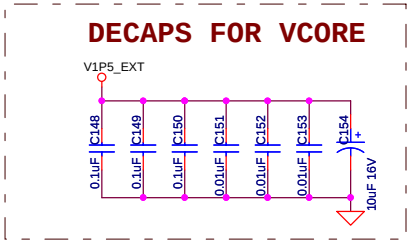
Actel		
Title: A2F-DEV-KIT		
Size: B	Document Number: PSRAM & FLASH I/F'S	Rev: F
Date: Tuesday, March 30, 2010	Sheet 24 of 35	

AGL 125 CS289 PWR/GND





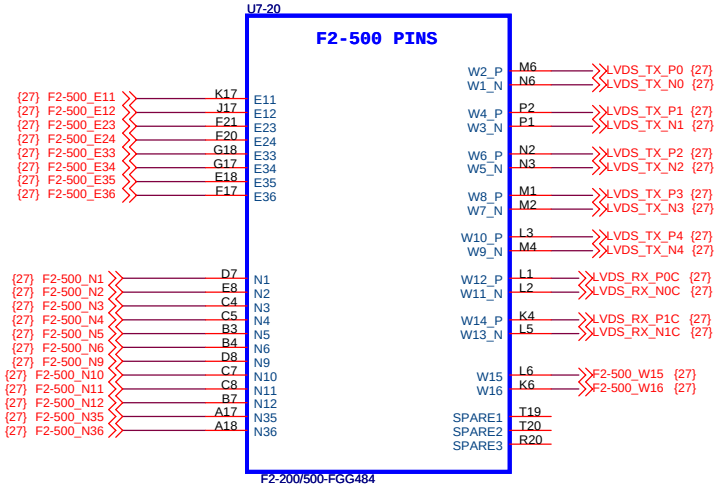




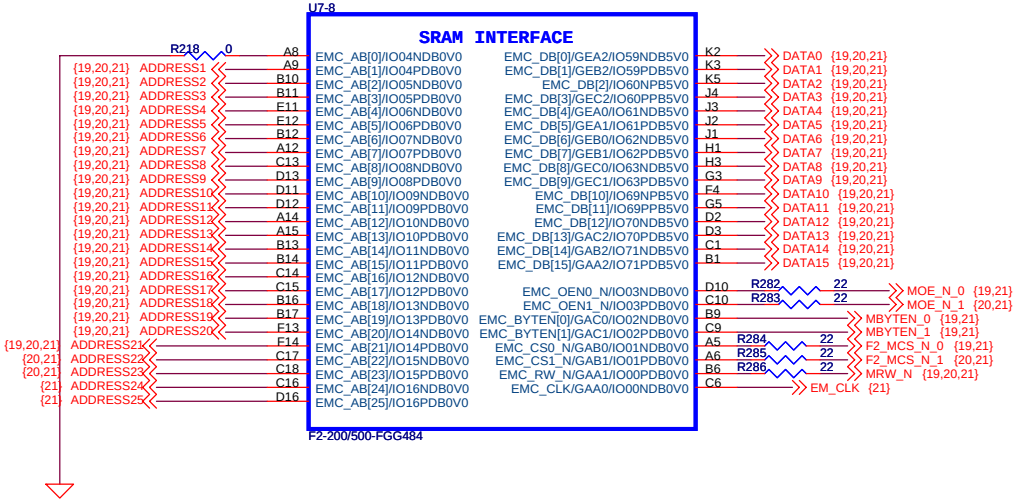
Actel

Actel		
Title: A2F-DEV-KIT		
Size: B	Document Number: AGL 125 CS289 PWR/GND	Rev: F
Date: Tuesday, March 30, 2010	Sheet 25 of 35	

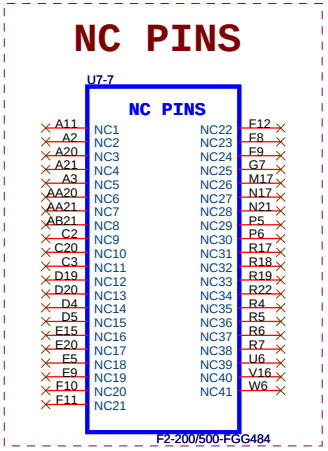
F2-500 PINS



MEMORY INTERFACE



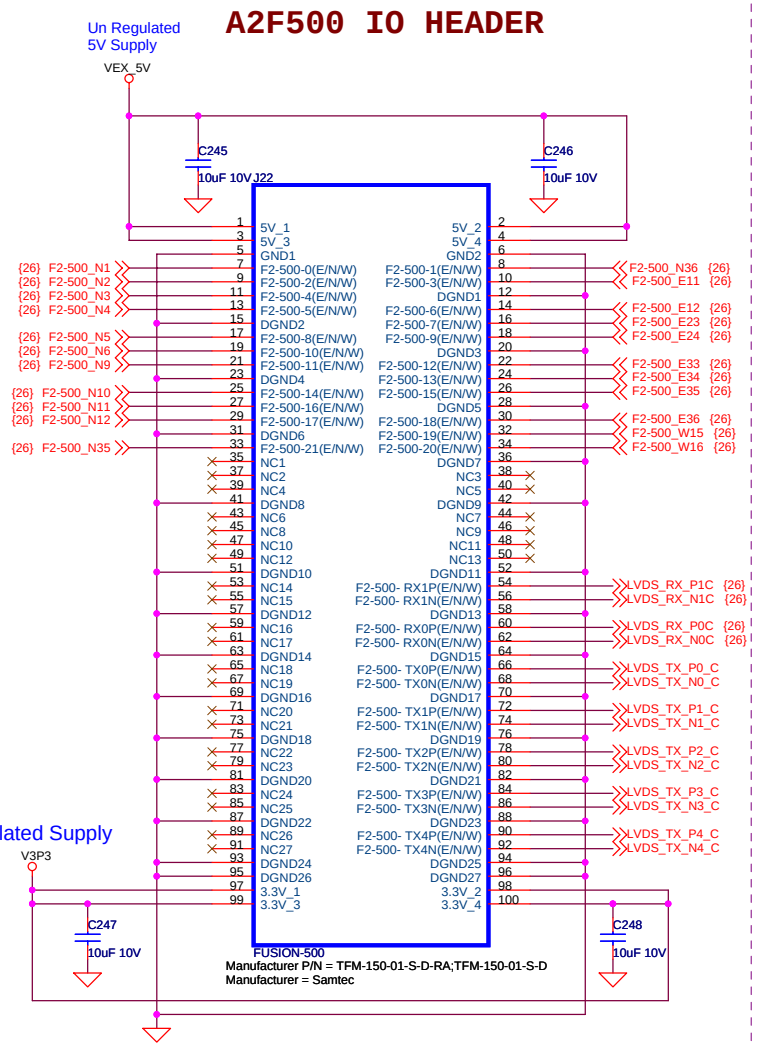
NC PINS



Actel			
Title: A2F-DEV-KIT			
Size: B	Document Number: F2-500, MEMORY & NC PINS		Rev: F
Date: Tuesday, March 30, 2010	Sheet 26 of 35		

F2-500 CONN & DIRECTC

A2F500 IO HEADER

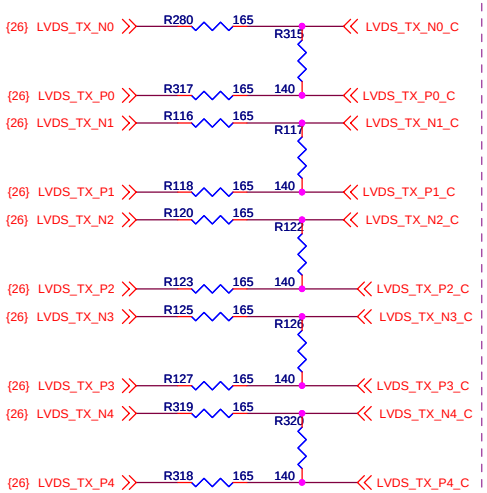


F2-500 CONNECTOR

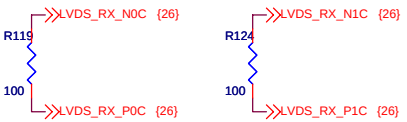
Vertical connector " TFM-150-01-S-D" can also be mounted on this foot print

LVDS_TX_TERMINATION

PLACE THESE COMPONENTS CLOSE TO FPGA

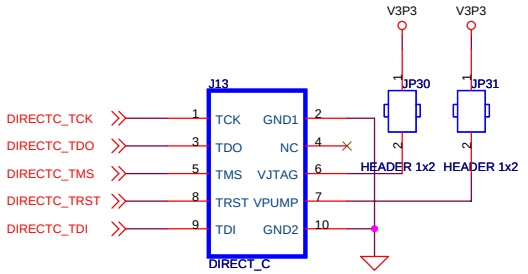


LVDS_RX TERMINATION

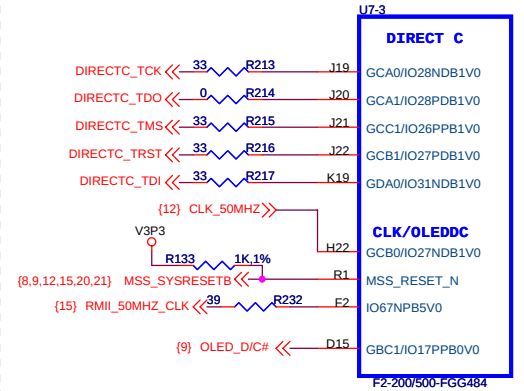


PLACE THESE COMPONENTS CLOSE TO FPGA

Direct C Programming



MANUFACTURER P/N = HTST-105-01-L-DV-A
MANUFACTURER = Samtec Inc



Actel

Title	A2F-DEV-KIT	
Size B	Document Number F2-500 CONN & DIRECTC	Rev F
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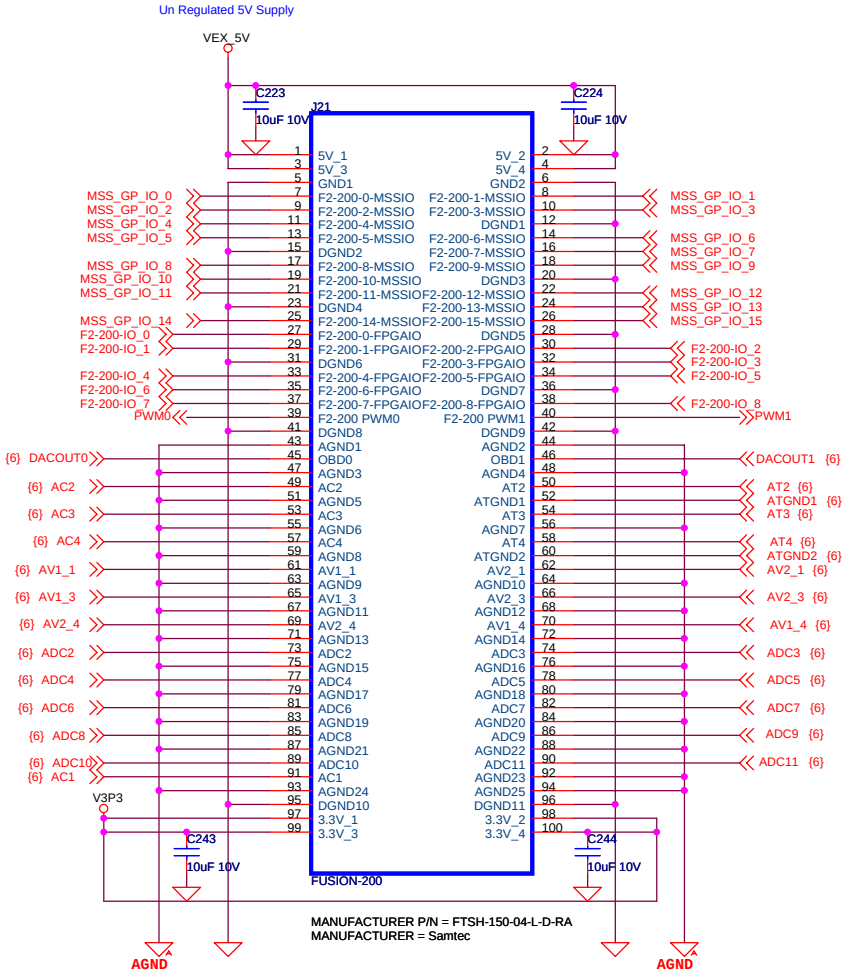
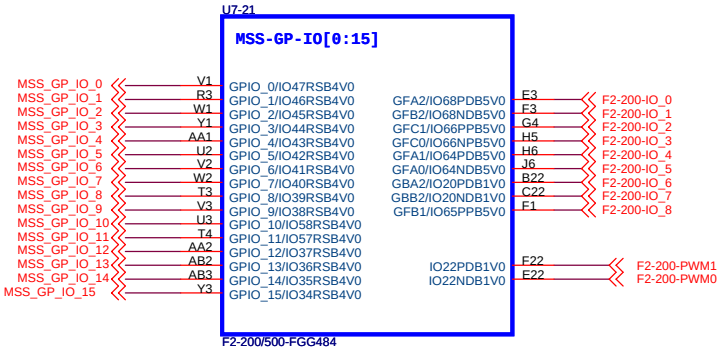
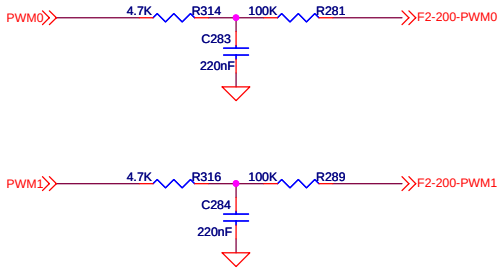
MIXED SIGNAL CONNECTOR



Matting connector " CLP-150-02-L-DH"



CORE PWM



Actel

Title: A2F-DEV-KIT

Size: B | Document Number: MIXED SIGNAL CONNECTOR | Rev: F

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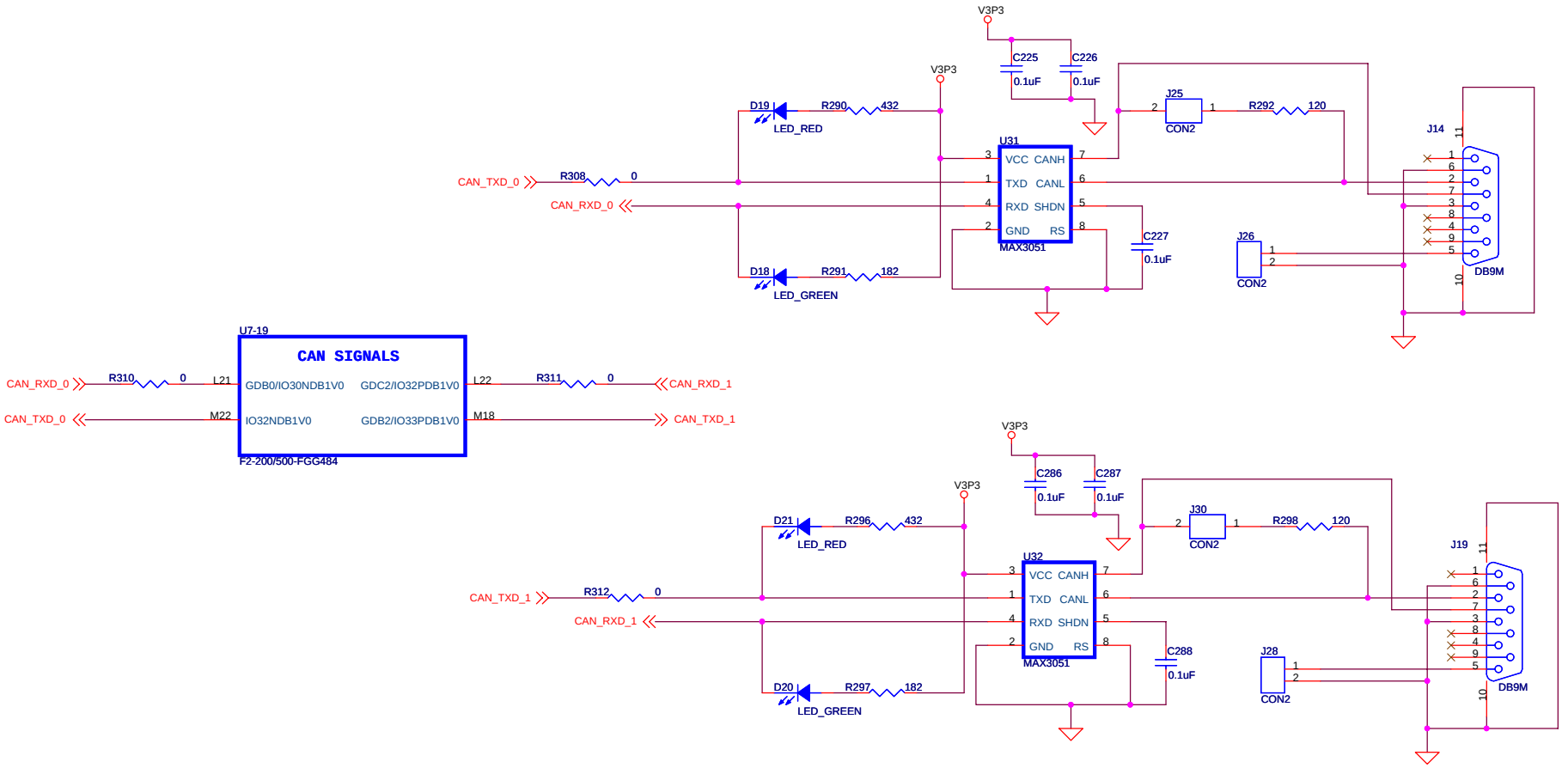
CAN INTERFACE



Actel

Title: A2F-DEV-KIT

Size	Document Number	Rev
B	CAN INTERFACE	F

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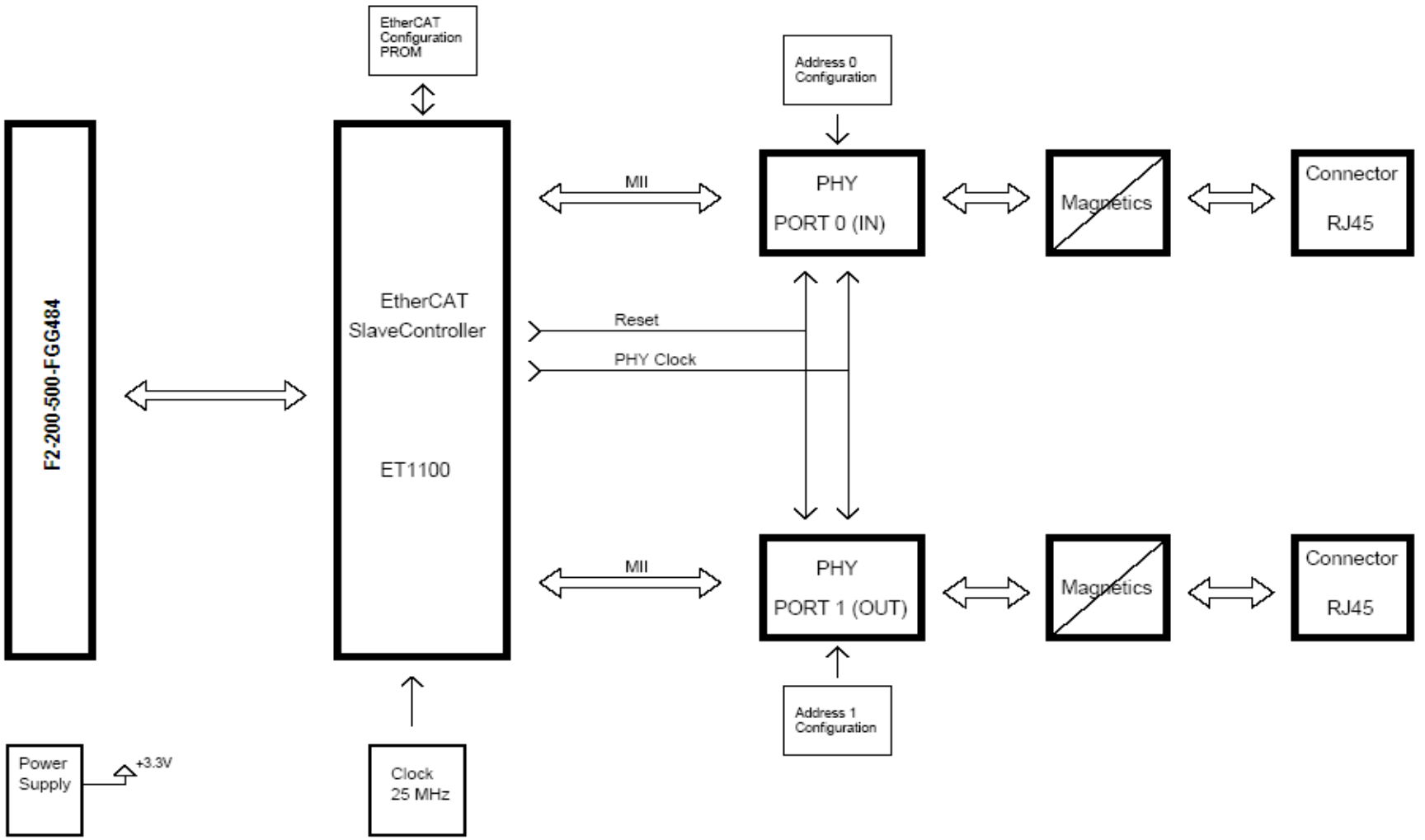


Actel

Title: A2F-DEV-KIT		
Size: A	Document Number: ETHER CAT BLOCK DIAGRAM	Rev: F
Date: Tuesday, March 30, 2010	Sheet 30 of 35	

Place R363 alone close to U55

U55A

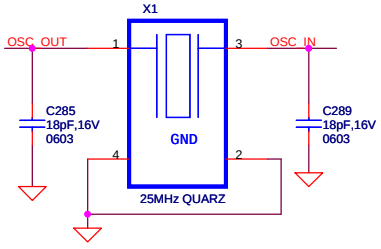
ET1100

U7-22

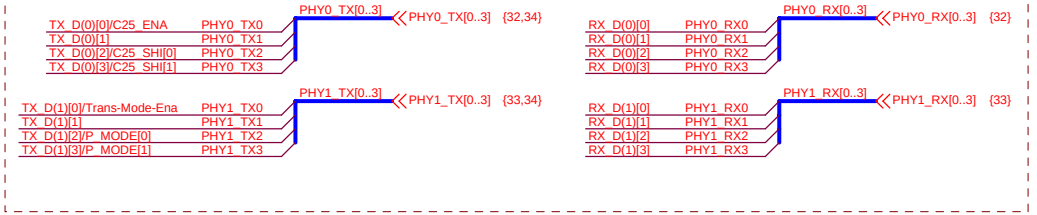
F2-200/500-FGG484

TP_VIA

Clock Distribution



TX/RX Signals for Ethercat Ports 0 to 1



Actel

Title	A2F-DEV-KIT
Size B / Document Number	ETHER CAT INTERFACE
Rev	F
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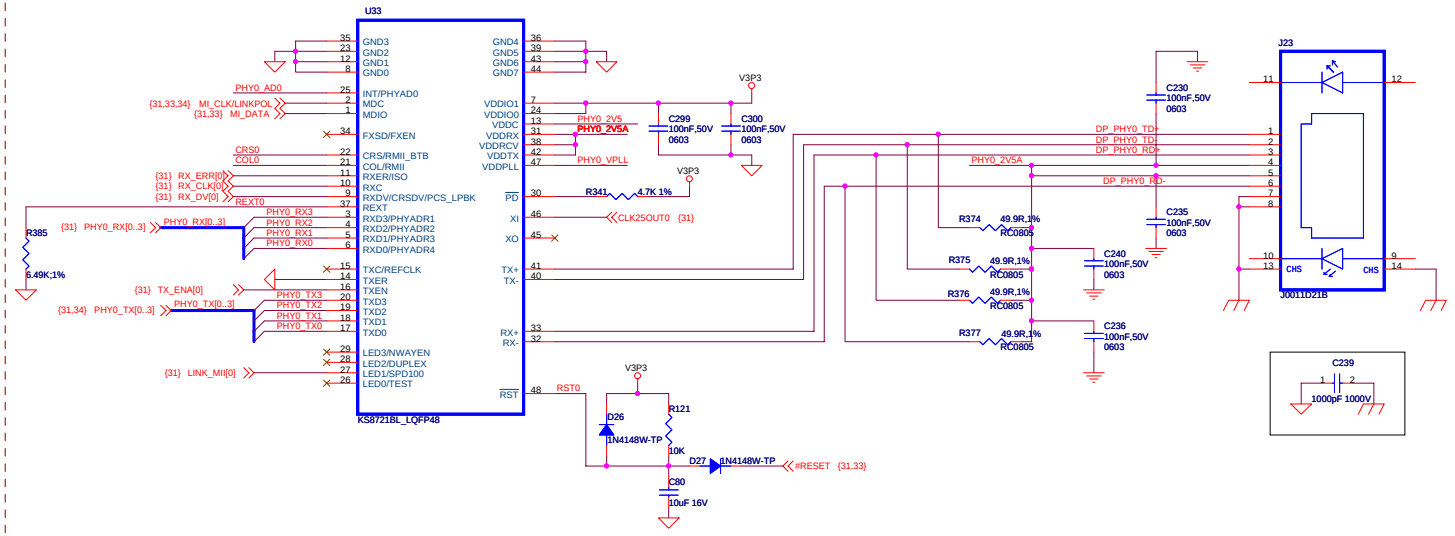
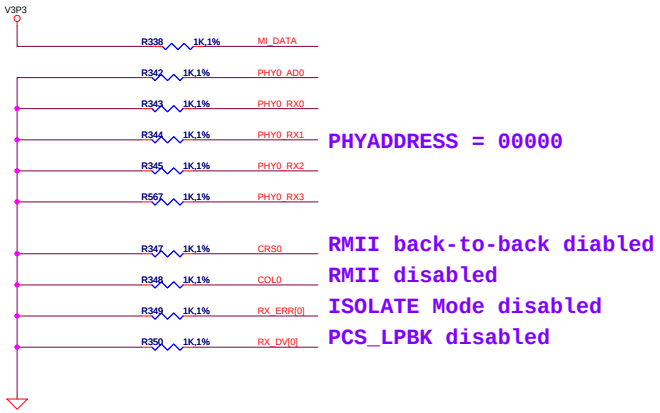
ETHER CAT PORT 0





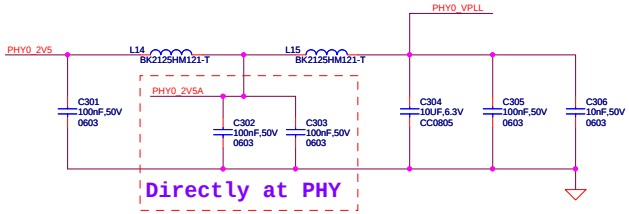
PHYADDRESS = 00000

RMII back-to-back diabled

RMII disabled

ISOLATE Mode disabled

PCS_LPBK disabled



Actel

Actel		
Title: A2F-DEV-KIT		
Size: C	Document Number: ETHER CAT PORT 0	Rev: F
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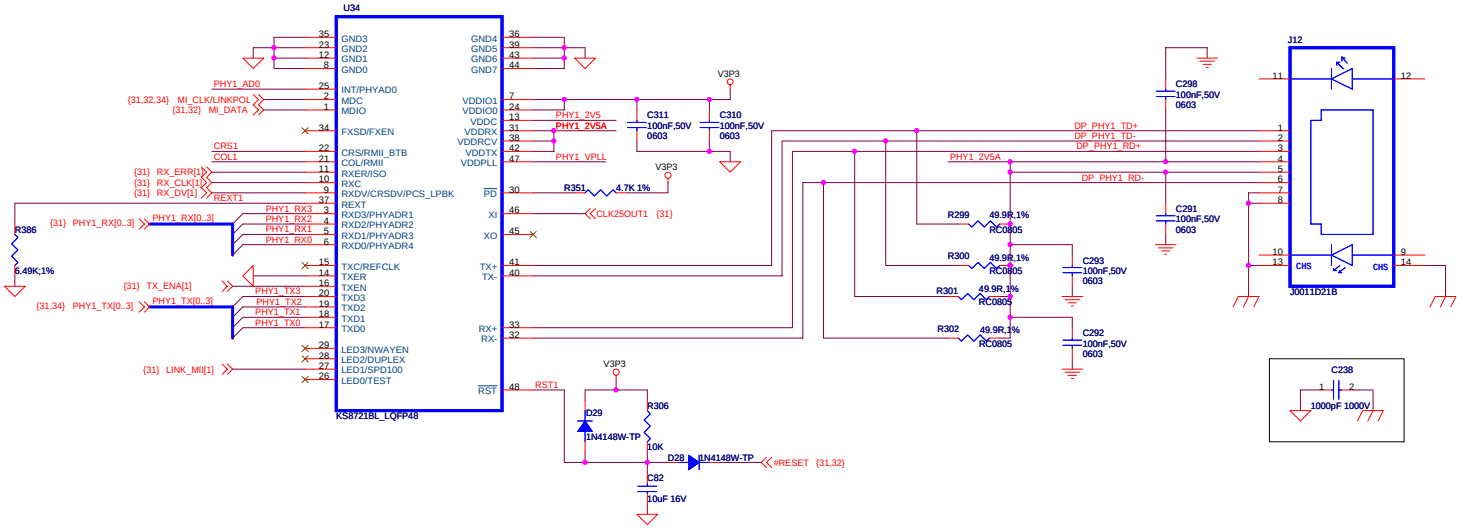
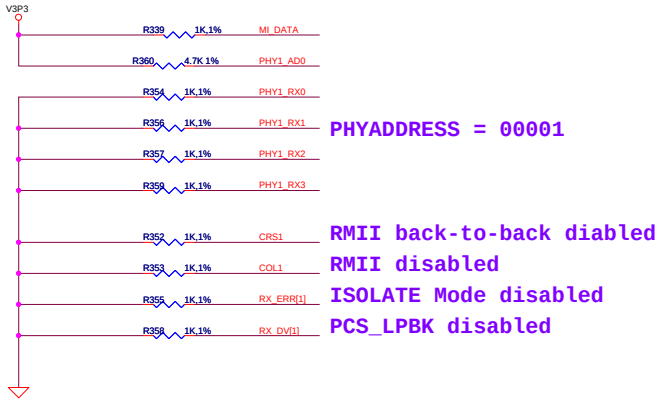
ETHER CAT PORT 1





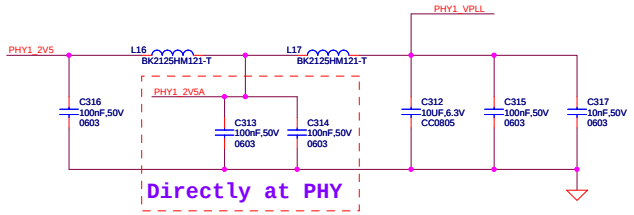
PHYADDRESS = 00001

RMII back-to-back diabled

RMII disabled

ISOLATE Mode disabled

PCS_LPBK disabled



Actel

Actel		
Title: A2F-DEV-KIT		
Size: C	Document Number: ETHER CAT PORT 1	Rev: F
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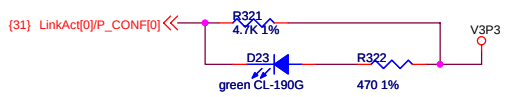
The Link/Activity-LED must be located either in the RJ45 connector
or directly besides the connector of the IN-Port.

No LEDs have to be connected to the PHYs!

Link/Activity Port_0



POR Value:
P_CONF[0]= 1 (Port0 = MII)

The Link/Activity-LED must be located either in the RJ45 connector
or directly besides the connector of the IN-Port.

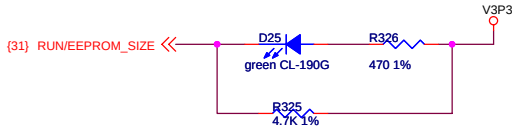
No LEDs have to be connected to the PHYs!

Link/Activity Port_1

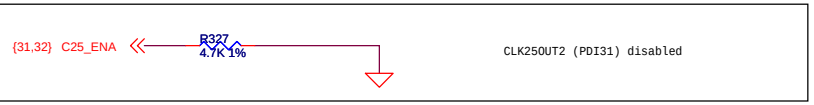
POR Value:
P_CONF[1]= 1 (Port1 = MII)

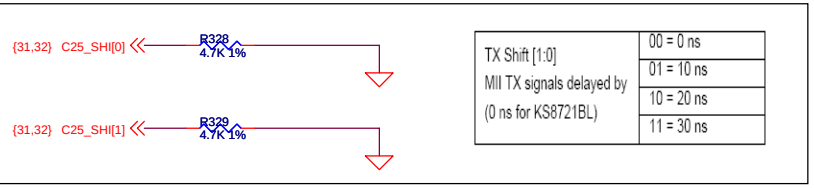
The RUN-LED shall be viewable without removing covers or parts from the devices

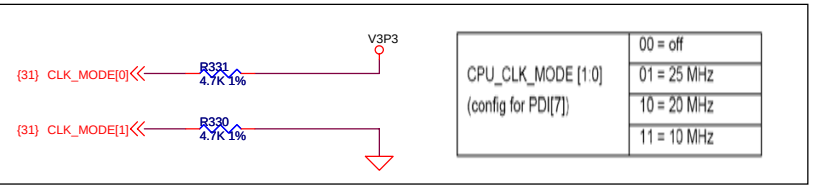
RUN/E²PROM-Size

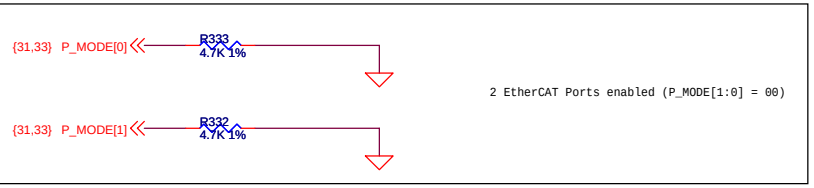


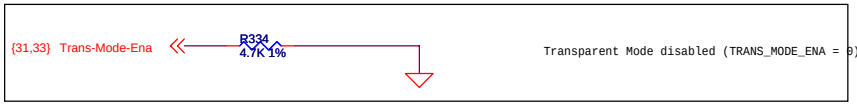
POR Value:
E²PPROM-Size = 0 (16 kBit)

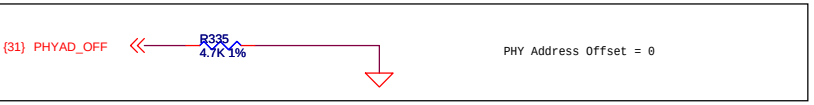


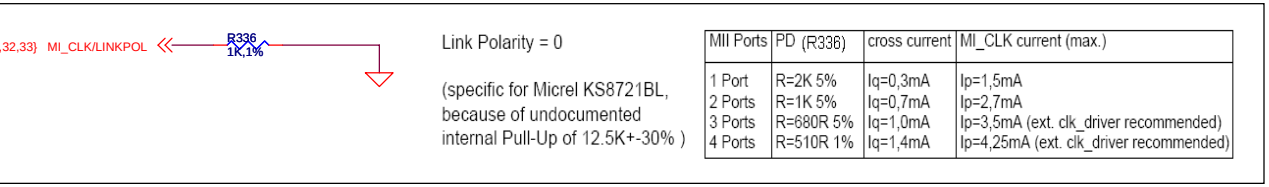












MII Ports	PD (R336)	cross current	MI_CLK current (max.)
1 Port	R=2K 5%	Iq=0,3mA	Ip=1,5mA
2 Ports	R=1K 5%	Iq=0,7mA	Ip=2,7mA
3 Ports	R=680R 5%	Iq=1,0mA	Ip=3,5mA (ext. clk_driver recommended)
4 Ports	R=510R 1%	Iq=1,4mA	Ip=4,25mA (ext. clk_driver recommended)

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Title: A2F-DEV-KIT

Size: B | Document Number: ETHER CAT LEDS & CONFIG | Rev: F

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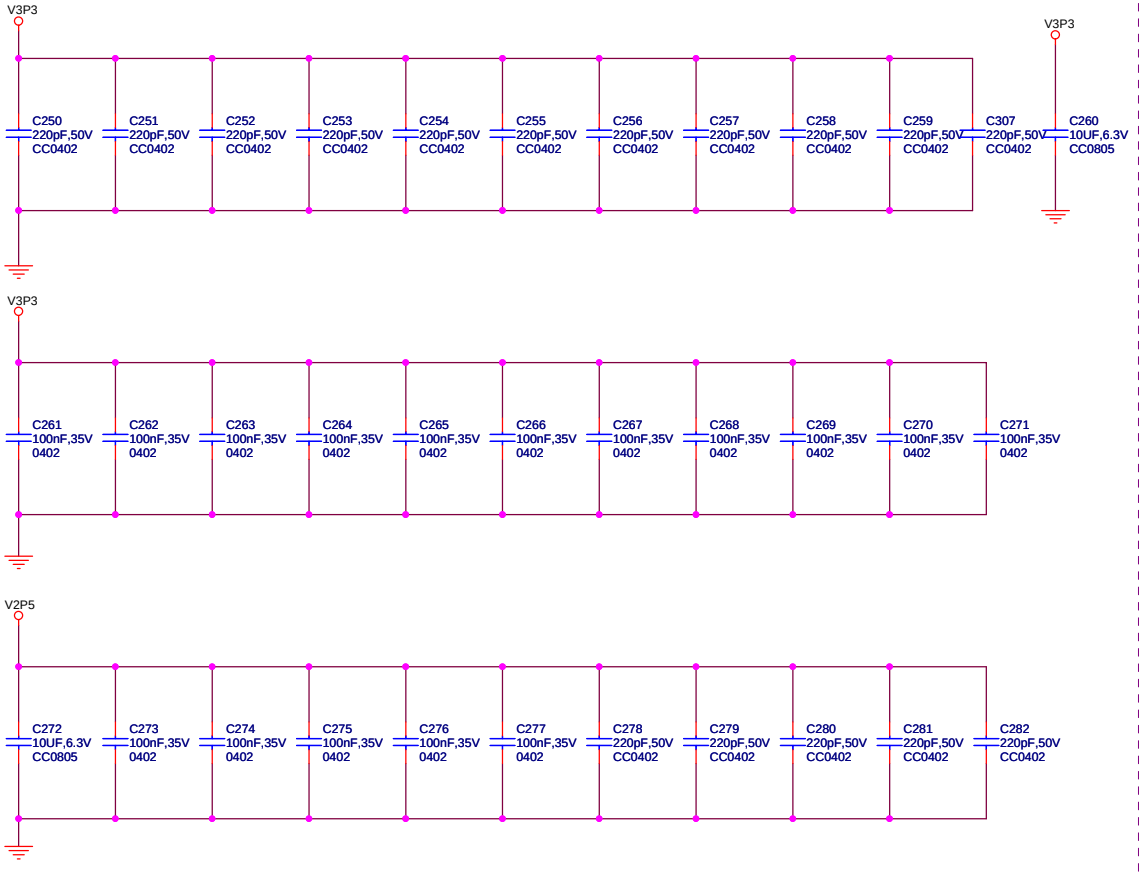
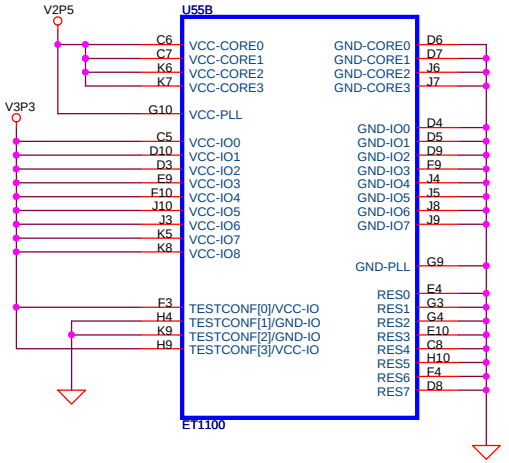
EHTER CAT DECAPS





Actel

Title: A2F-DEV-KIT		
Size: B	Document Number: ETHER CAT PWR & GND	Rev: F
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